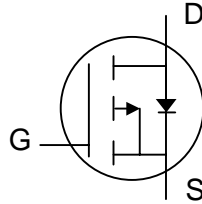


P-channel Enhancement-mode Power MOSFET

- Simple drive requirement
- Lower gate charge
- Fast switching characteristics



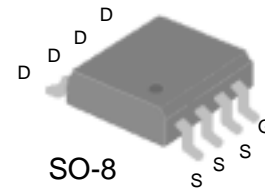
| | |
|--------------|---------------|
| BV_{DSS} | -80V |
| $R_{DS(ON)}$ | 180m Ω |
| I_D | -2.7A |

 **Pb-free; RoHS compliant.**

DESCRIPTION

Advanced Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SSM9585GM is in the SO-8 package, which is widely preferred for commercial and industrial surface mount applications. This device is suitable for low voltage applications such as DC/DC converters.



ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Rating | Units |
|------------------------------|---------------------------------------|------------|---------------------|
| V_{DS} | Drain-Source Voltage | -80 | V |
| V_{GS} | Gate-Source Voltage | ± 25 | V |
| $I_D @ T_A=25^\circ\text{C}$ | Continuous Drain Current ³ | -2.7 | A |
| $I_D @ T_A=70^\circ\text{C}$ | Continuous Drain Current ³ | -2.1 | A |
| I_{DM} | Pulsed Drain Current ¹ | -20 | A |
| $P_D @ T_A=25^\circ\text{C}$ | Total Power Dissipation | 2.5 | W |
| | Linear Derating Factor | 0.02 | W/ $^\circ\text{C}$ |
| T_{STG} | Storage Temperature Range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ\text{C}$ |

THERMAL DATA

| Symbol | Parameter | Value | Unit |
|------------------|--|-------|---------------------------|
| $R_{\theta j-a}$ | Maximum Thermal Resistance Junction-ambient ³ | 50 | $^\circ\text{C}/\text{W}$ |

ELECTRICAL CHARACTERISTICS (at $T_j = 25^\circ\text{C}$, unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|------------------------------|---|---|------|-------|-----------|---------------------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=-250\mu A$ | -80 | - | - | V |
| $\Delta BV_{DSS}/\Delta T_j$ | Breakdown Voltage Temperature Coefficient | Reference to 25°C , $I_D=-1\text{mA}$ | - | -0.07 | - | V/ $^\circ\text{C}$ |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance ² | $V_{GS}=-10V, I_D=-2.7A$ | - | - | 180 | m Ω |
| | | $V_{GS}=-4.5V, I_D=-2.5A$ | - | - | 200 | m Ω |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}, I_D=-250\mu A$ | -1 | - | -3 | V |
| g_{fs} | Forward Transconductance | $V_{DS}=-10V, I_D=-2.7A$ | - | 5 | - | S |
| I_{DSS} | Drain-Source Leakage Current ($T_j=25^\circ\text{C}$) | $V_{DS}=-80V, V_{GS}=0V$ | - | - | -1 | μA |
| | Drain-Source Leakage Current ($T_j=70^\circ\text{C}$) | $V_{DS}=-64V, V_{GS}=0V$ | - | - | -25 | μA |
| I_{GSS} | Gate-Source Leakage | $V_{GS}=\pm 25V$ | - | - | ± 100 | nA |
| Q_g | Total Gate Charge ² | $I_D=-2.7A$ | - | 18 | 28 | nC |
| Q_{gs} | Gate-Source Charge | $V_{DS}=-64V$ | - | 5 | - | nC |
| Q_{gd} | Gate-Drain ("Miller") Charge | $V_{GS}=-4.5V$ | - | 7 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time ² | $V_{DS}=-40V$ | - | 10 | - | ns |
| t_r | Rise Time | $I_D=-1A$ | - | 6 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | $R_G=3.3\Omega, V_{GS}=-10V$ | - | 67 | - | ns |
| t_f | Fall Time | $R_D=40\Omega$ | - | 30 | - | ns |
| C_{iss} | Input Capacitance | $V_{GS}=0V$ | - | 1790 | 2860 | pF |
| C_{oss} | Output Capacitance | $V_{DS}=-25V$ | - | 140 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | $f=1.0\text{MHz}$ | - | 98 | - | pF |

SOURCE-DRAIN DIODE

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|----------|------------------------------------|-------------------------|------|------|------|-------|
| V_{SD} | Forward On Voltage ² | $I_S=-2A, V_{GS}=0V$ | - | - | -1.2 | V |
| t_{rr} | Reverse Recovery Time ² | $I_S=-2.7A, V_{GS}=0V,$ | - | 80 | - | ns |
| Q_{rr} | Reverse Recovery Charge | $di/dt=100A/\mu s$ | - | 320 | - | nC |

Notes:

1. Pulse width limited by maximum junction temperature.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Surface-mounted on 1 in² copper pad on FR4 board; 125 $^\circ\text{C}/W$ when mounted on minimum copper pad.

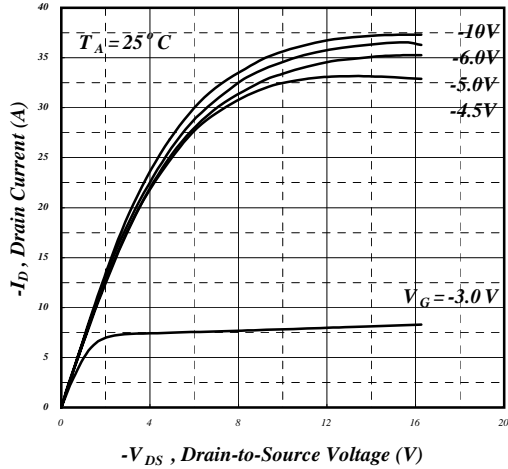


Fig 1. Typical Output Characteristics

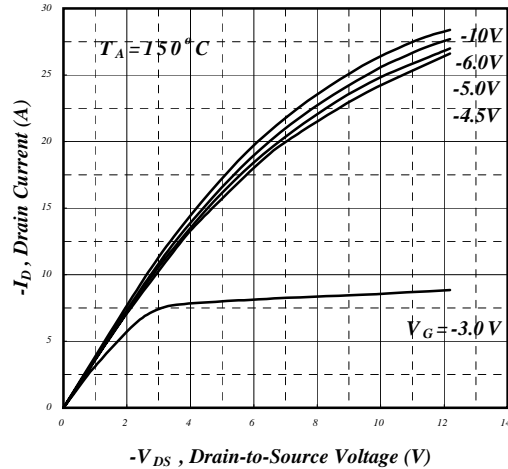


Fig 2. Typical Output Characteristics

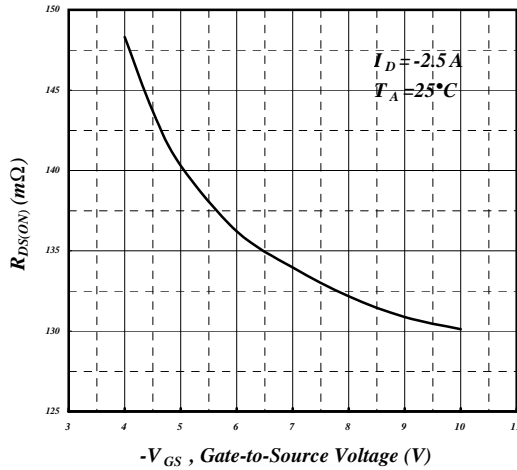


Fig 3. On-Resistance vs. Gate Voltage

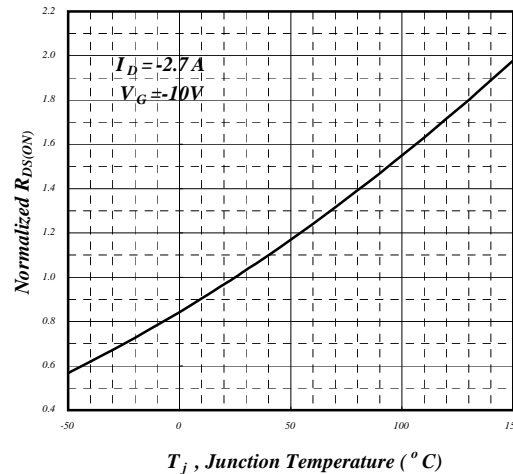


Fig 4. Normalized On-Resistance vs. Junction Temperature

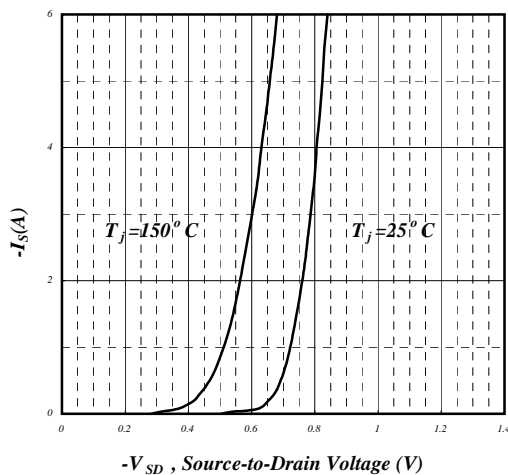


Fig 5. Forward Characteristic of Reverse Diode

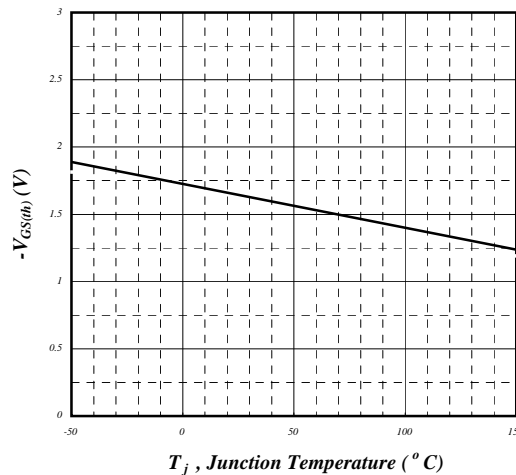


Fig 6. Gate Threshold Voltage vs. Junction Temperature

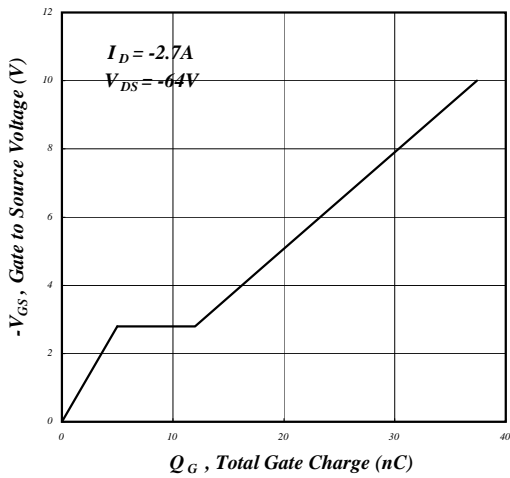


Fig 7. Gate Charge Characteristics

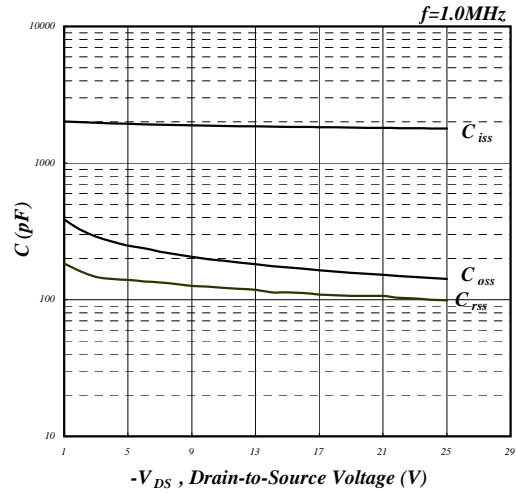


Fig 8. Typical Capacitance Characteristics

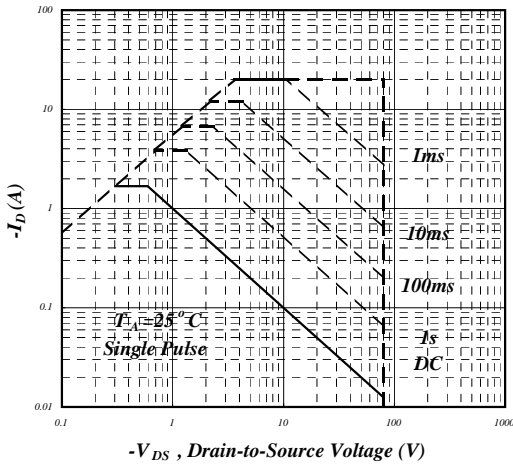


Fig 9. Maximum Safe Operating Area

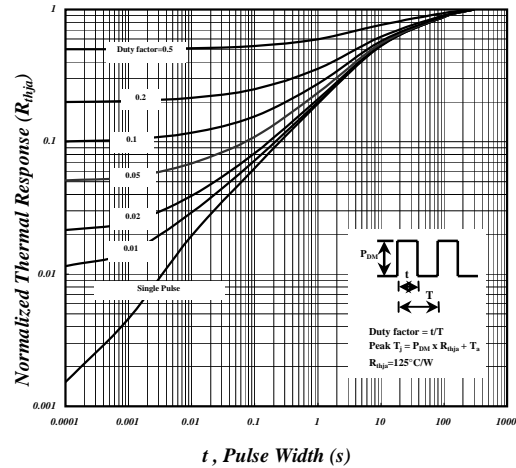


Fig 10. Effective Transient Thermal Impedance

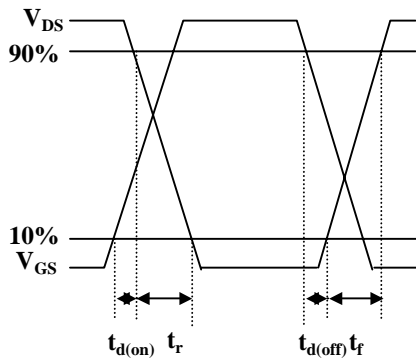


Fig 11. Switching Time Waveform

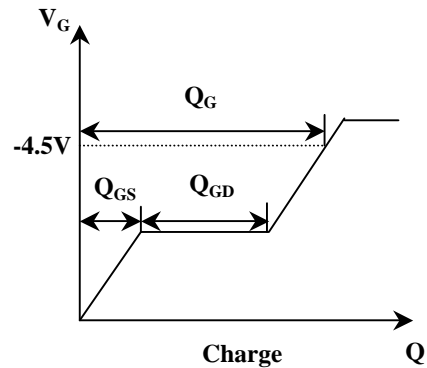


Fig 12. Gate Charge Waveform

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