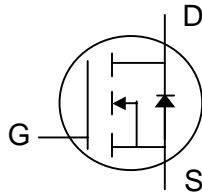


N-CHANNEL ENHANCEMENT-MODE POWER MOSFET

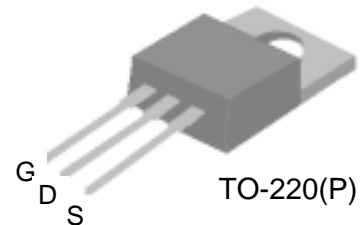
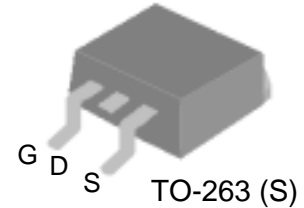
Low gate-charge
Simple drive requirement
Fast switching



BV_{DSS}	60V
$R_{DS(ON)}$	8.5m Ω
I_D	75A

Description

The SSM95T06S is in a TO-263 package, which is widely used for commercial and industrial surface mount applications, and is well suited for low voltage applications such as DC/DC converters. The through-hole version, the SSM95T06P in TO-220, is available for low-footprint vertical mounting. These devices are manufactured with an advanced process, providing improved on-resistance and switching performance.



 **Pb-free lead finish (second-level interconnect)**

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^3$	75	A
$I_D @ T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	66	A
I_{DM}	Pulsed Drain Current ¹	260	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	138	W
	Linear Derating Factor	1.11	W/ $^\circ\text{C}$
E_{AS}	Single Pulse Avalanche Energy ⁴	450	mJ
I_{AR}	Avalanche Current	30	A
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Thermal Resistance Junction-case	Max. 0.9	$^\circ\text{C}/\text{W}$
Rthj-a	Thermal Resistance Junction-ambient	Max. 62	$^\circ\text{C}/\text{W}$

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	60	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1mA$	-	0.05	-	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=45A$	-	-	8.5	$m\Omega$
		$V_{GS}=4.5V, I_D=20A$	-	-	12	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=45A$	-	72	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^{\circ}\text{C}$)	$V_{DS}=60V, V_{GS}=0V$	-	-	10	μA
	Drain-Source Leakage Current ($T_j=150^{\circ}\text{C}$)	$V_{DS}=48V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_D=45A$	-	72	115	nC
Q_{gs}	Gate-Source Charge	$V_{DS}=48V$	-	16	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	53	-	nC
$t_{d(on)}$	Turn-on Delay Time ²	$V_{DS}=30V$	-	20	-	ns
t_r	Rise Time	$I_D=45A$	-	76	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	67	-	ns
t_f	Fall Time	$R_D=0.67\Omega$	-	109	-	ns
C_{iss}	Input Capacitance	$V_{GS}=0V$	-	5700	9200	pF
C_{oss}	Output Capacitance	$V_{DS}=25V$	-	900	-	pF
C_{rss}	Reverse Transfer Capacitance	$f=1.0MHz$	-	560	-	pF
R_g	Gate Resistance	$f=1.0MHz$	-	1.1	1.7	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=45A, V_{GS}=0V$	-	-	1.3	V
t_{rr}	Reverse Recovery Time ²	$I_S=20A, V_{GS}=0V$	-	40	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	60	-	nC

Notes:

1. Pulse width limited by safe operating area.
2. Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. The maximum current is limited by the package to 75A.
4. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=30V$, $L=1mH$, $R_G=25\Omega$, $I_{AS}=30A$.

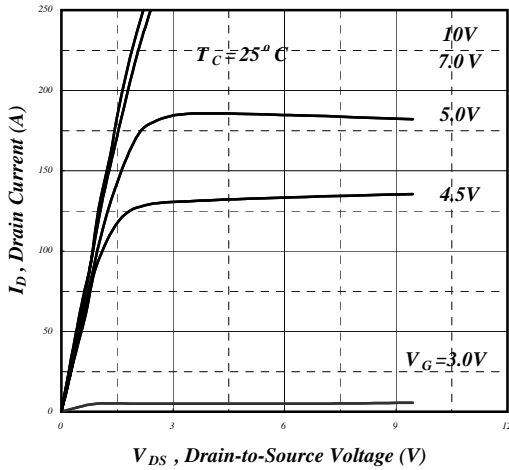


Fig 1. Typical Output Characteristics

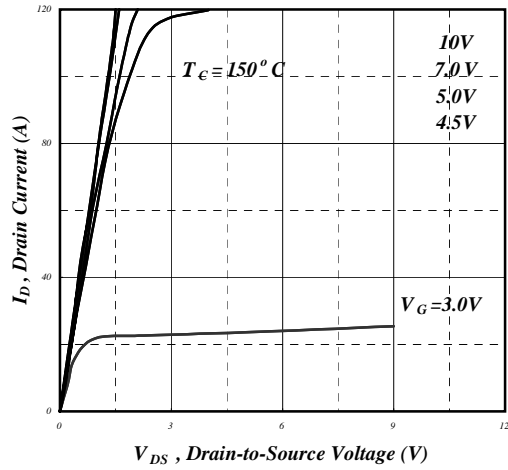


Fig 2. Typical Output Characteristics

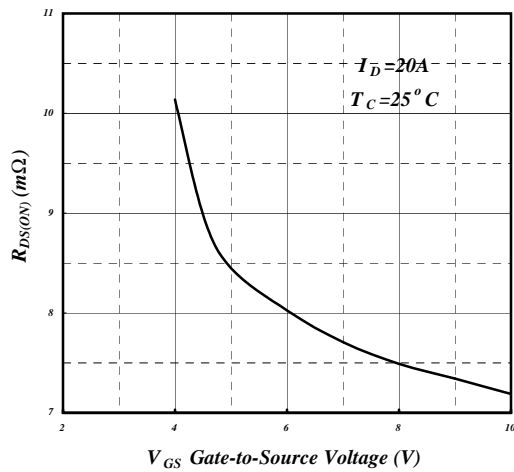


Fig 3. On-Resistance vs. Gate Voltage

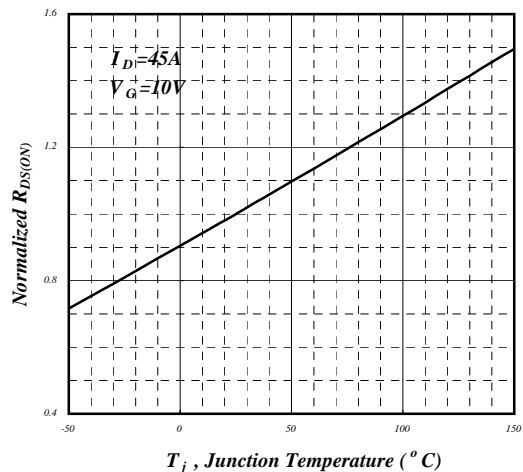


Fig 4. Normalized On-Resistance vs. Junction Temperature

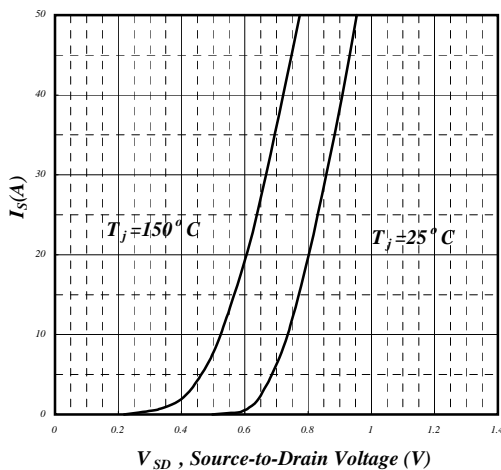


Fig 5. Forward Characteristic of Reverse Diode

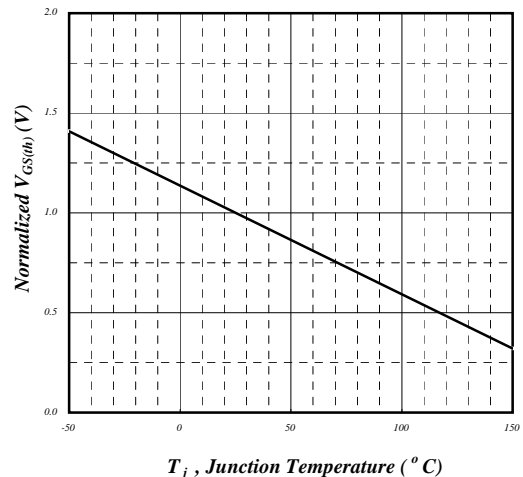


Fig 6. Gate Threshold Voltage vs. Junction Temperature

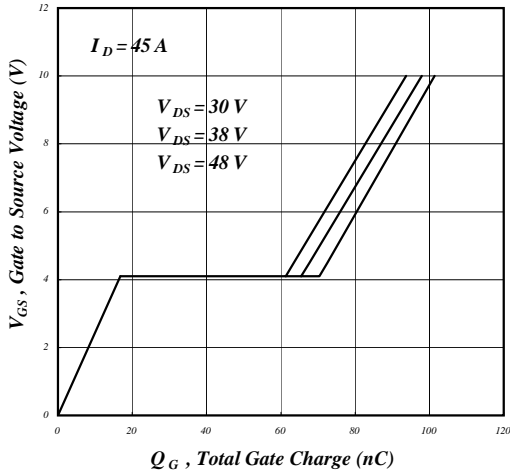


Fig 7. Gate Charge Characteristics

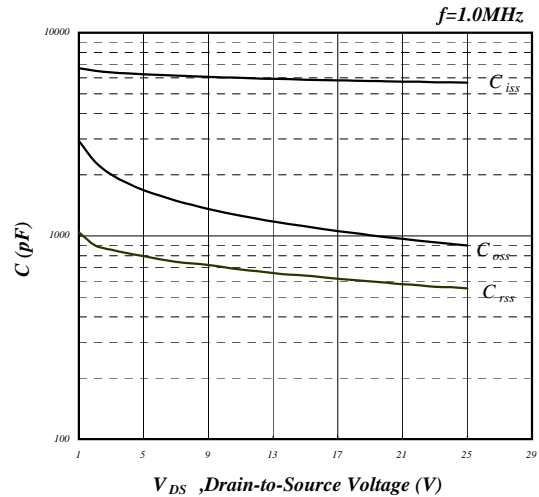


Fig 8. Typical Capacitance Characteristics

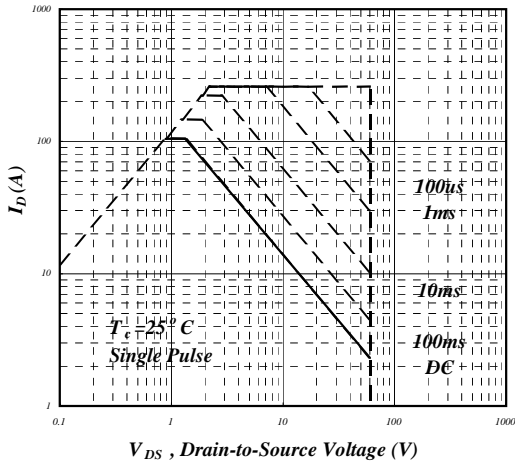


Fig 9. Maximum Safe Operating Area

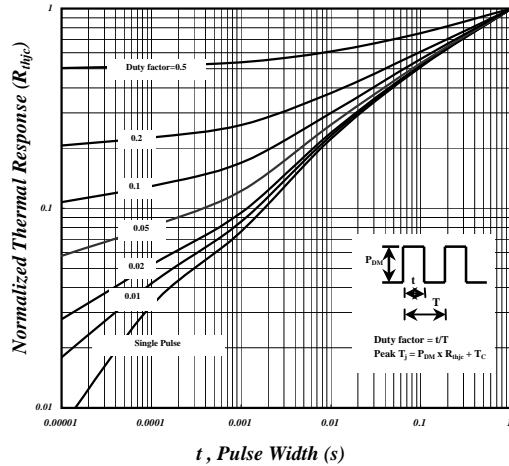


Fig 10. Effective Transient Thermal Impedance

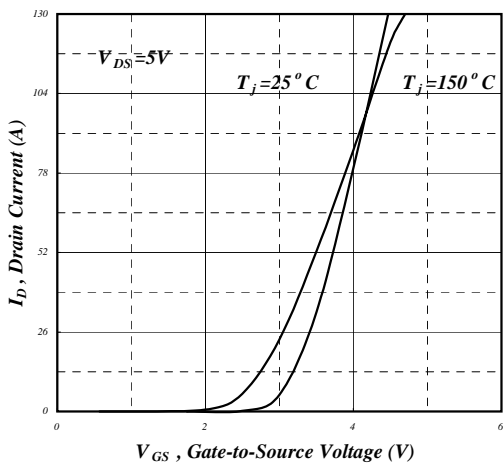


Fig 11. Transfer Characteristics

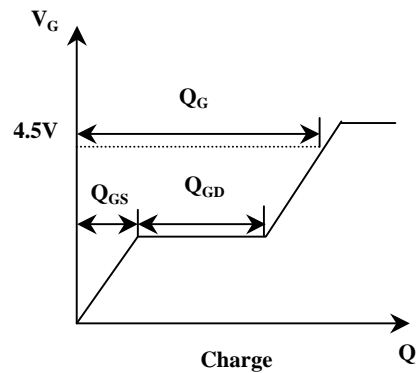


Fig 12. Gate Charge Waveform

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