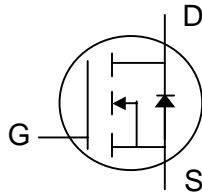


## N-CHANNEL ENHANCEMENT-MODE POWER MOSFET

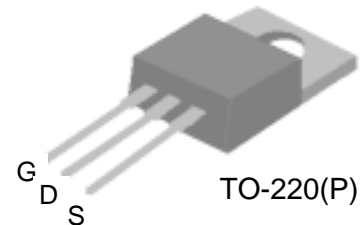
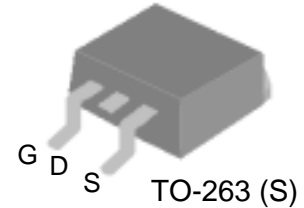
Low gate-charge  
Simple drive requirement  
Fast switching



$V_{DS}$	60V
$R_{DS(ON)}$	18m $\Omega$
$I_D$	60A

### Description

The SSM9972GS is in a TO-263 package, which is widely used for commercial and industrial surface mount applications, and is well suited for low voltage applications such as DC/DC converters. The through-hole version, the SSM9972GP in TO-220, is available for low-footprint vertical mounting. These devices are manufactured with an advanced process, providing improved on-resistance and switching performance.



 **Pb-free lead finish (second-level interconnect)**

### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	60	V
$V_{GS}$	Gate-Source Voltage	$\pm 25$	V
$I_D @ T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^3$	60	A
$I_D @ T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10V$	38	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	230	A
$P_D @ T_C=25^\circ\text{C}$	Total Power Dissipation	89	W
	Linear Derating Factor	0.7	W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Thermal Resistance Junction-case	Max. 1.4	$^\circ\text{C}/\text{W}$
Rthj-a	Thermal Resistance Junction-ambient	Max. 62	$^\circ\text{C}/\text{W}$

**Electrical Characteristics @ T<sub>j</sub>=25°C (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	-	-	V
ΔBV <sub>DSS</sub> / ΔT <sub>j</sub>	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I <sub>D</sub> =1mA	-	0.06	-	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =35A	-	-	18	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =25A	-	-	22	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =35A	-	55	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	V <sub>DS</sub> =60V, V <sub>GS</sub> =0V	-	-	10	uA
	Drain-Source Leakage Current (T <sub>j</sub> =150°C)	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> =±25V	-	-	±100	nA
Q <sub>g</sub>	Total Gate Charge <sup>2</sup>	I <sub>D</sub> =35A	-	32	51	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =48V	-	8	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =4.5V	-	20	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time <sup>2</sup>	V <sub>DS</sub> =30V	-	11	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =35A	-	58	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =3.3Ω, V <sub>GS</sub> =10V	-	45	-	ns
t <sub>f</sub>	Fall Time	R <sub>D</sub> =0.86Ω	-	80	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	3170	5070	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =25V	-	280	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	230	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	1.7	-	Ω

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =35A, V <sub>GS</sub> =0V	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =35A, V <sub>GS</sub> =0V,	-	50	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	-	48	-	nC

**Notes:**

- 1.Pulse width limited by max. junction temperature.
- 2.Pulse width ≤300us , duty cycle ≤2%.

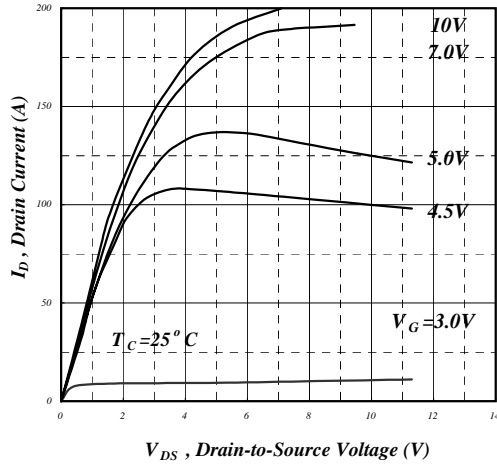


Fig 1. Typical Output Characteristics

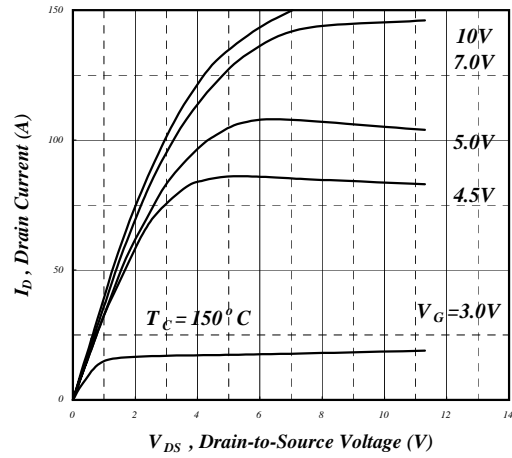


Fig 2. Typical Output Characteristics

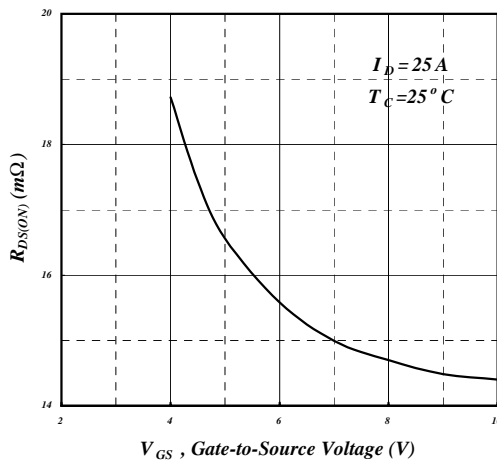


Fig 3. On-Resistance v.s. Gate Voltage

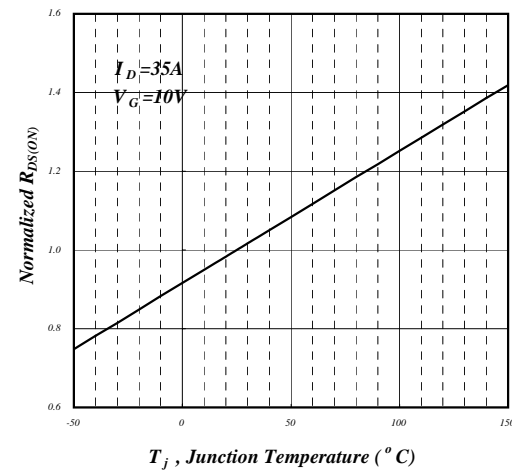


Fig 4. Normalized On-Resistance vs. Junction Temperature

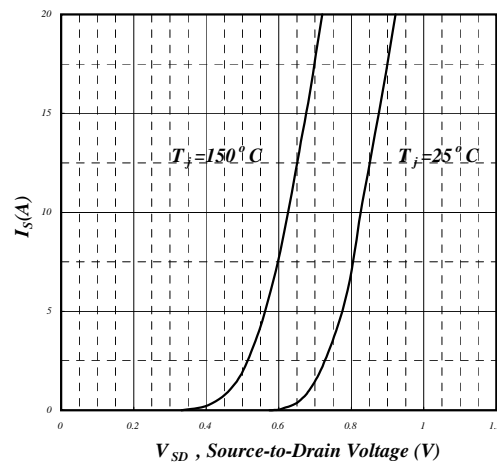


Fig 5. Forward Characteristic of Reverse Diode

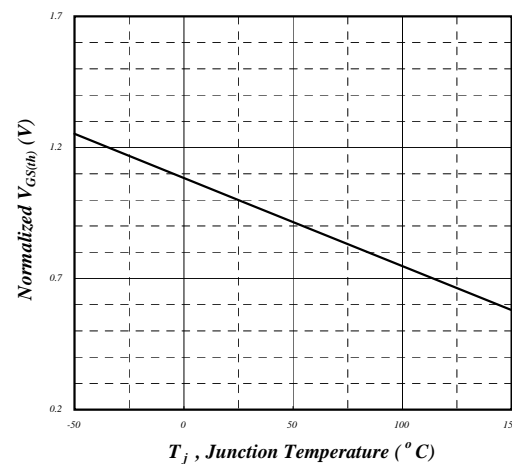


Fig 6. Gate Threshold Voltage vs. Junction Temperature

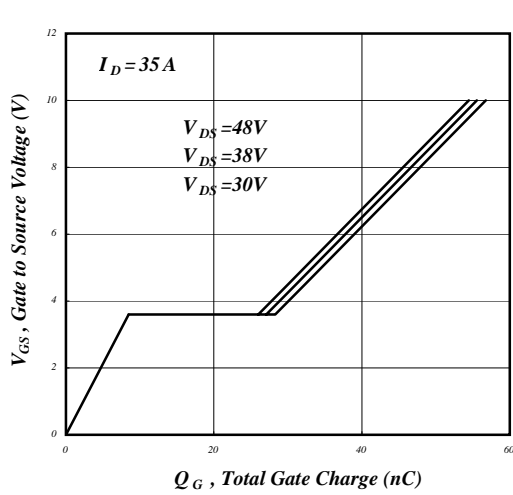


Fig 7. Gate Charge Characteristics

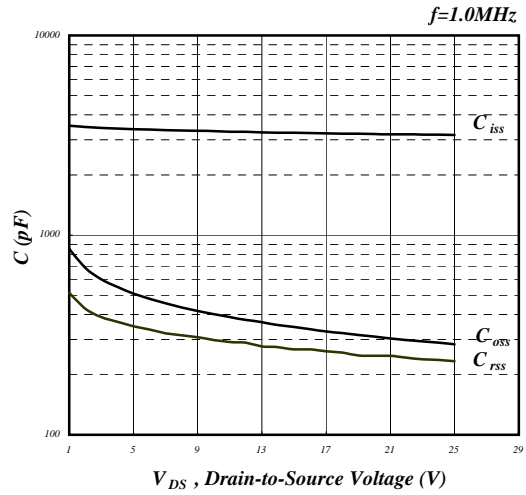


Fig 8. Typical Capacitance Characteristics

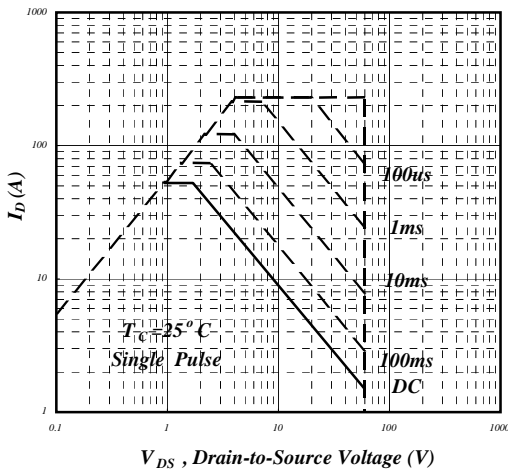


Fig 9. Maximum Safe Operating Area

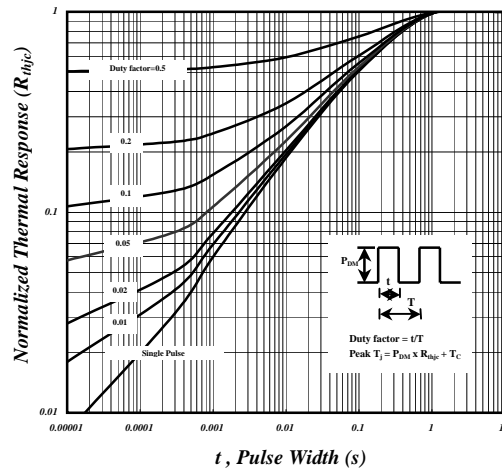


Fig 10. Effective Transient Thermal Impedance

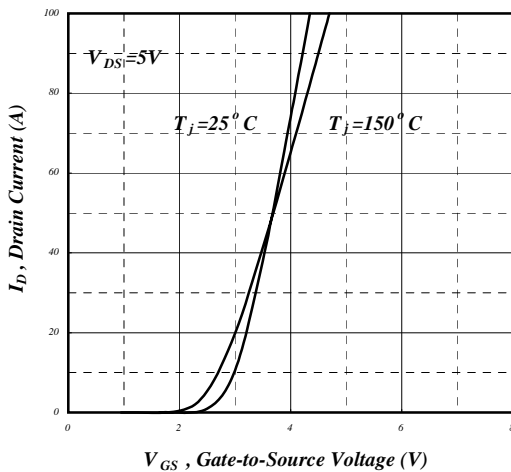


Fig 11. Transfer Characteristics

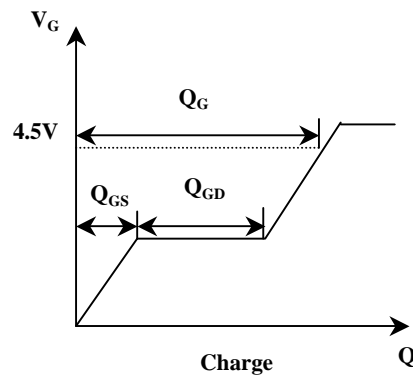


Fig 12. Gate Charge Waveform

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