# Normally – OFF Silicon Carbide Junction Transistor

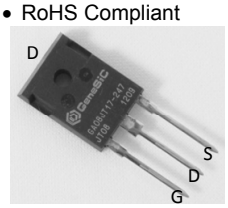
| | | |
|---|---|---|
| $V_{DS}$ | = | 1700 V |
| $V_{DS(ON)}$ | = | 1.8 V |
| $I_D$ | = | 8 A |
| $R_{DS(ON)}$ | = | 230 mΩ |

## Features

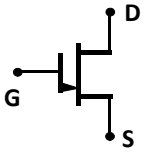
- 175 °C maximum operating temperature
- Temperature independent switching performance
- Gate oxide free SiC switch
- Suitable for connecting an anti-parallel diode
- Positive temperature coefficient for easy paralleling
- Low gate charge
- Low intrinsic capacitance

## Package

- RoHS Compliant




TO-247AB




## Advantages

- SiC transistor most compatible with existing Si gate-drivers
- Low switching losses
- Higher efficiency
- High temperature operation
- High short circuit withstand capability

## Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

## Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Values | Unit |
|---|---|---|---|---|
| Drain – Source Voltage | $V_{DS}$ | $V_{GS}$ = 0 V | 1700 | V |
| Continuous Drain Current | $I_D$ | $T_{C,MAX}$ = 90 °C | 8 | A |
| Gate Peak Current | $I_{GM}$ | | 5 | A |
| Turn-Off Safe Operating Area | RBSOA | $T_{VJ}$ = 175 °C, $I_G$ = 1 A, Clamped Inductive Load | $I_{D,max}$ = 8 @ $V_{DS} \le V_{DSmax}$ | A |
| Short Circuit Safe Operating Area | SCSOA | $T_{VJ}$ = 175 °C, $I_G$ = 1 A, $V_{DS}$ = 1200 V, Non Repetitive | 20 | µs |
| Reverse Gate – Source Voltage | $V_{SG}$ | | 30 | V |
| Reverse Drain – Source Voltage | $V_{SD}$ | | 50 | V |
| Power Dissipation | $P_{tot}$ | $T_C$ = 25 °C | 146 | W |
| Storage Temperature | $T_{stg}$ | | -55 to 175 | °C |

## Electrical Characteristics

| Parameter | Symbol | Conditions | Values min. | Values typ. | Values max. | Unit |
|---|---|---|---|---|---|---|
| **On Characteristics** | | | | | | |
| Drain – Source On Voltage | $V_{DS(ON)}$ | $I_D$ = 8 A, $I_G$ = 500 mA, $T_j$ = 25 °C | | 1.8 | 2.3 | V |
| | | $I_D$ = 8 A, $I_G$ = 1000 mA, $T_j$ = 125 °C | | 3.3 | 4.0 | |
| | | $I_D$ = 8 A, $I_G$ = 1000 mA, $T_j$ = 175 °C | | 4.5 | 5.5 | |
| Drain – Source On Resistance | $R_{DS(ON)}$ | $I_D$ = 8 A, $I_G$ = 500 mA, $T_j$ = 25 °C | | 230 | | mΩ |
| | | $I_D$ = 8 A, $I_G$ = 1000 mA, $T_j$ = 125 °C | | 410 | | |
| | | $I_D$ = 8 A, $I_G$ = 1000 mA, $T_j$ = 175 °C | | 560 | | |
| Gate Forward Voltage | $V_{GS(FWD)}$ | $I_G$ = 500 mA, $T_j$ = 25 °C | | 3.0 | | V |
| | | $I_G$ = 500 mA, $T_j$ = 175 °C | | 2.8 | | |
| DC Current Gain | β | $V_{DS}$ = 5 V, $I_D$ = 8 A, $T_j$ = 25 °C | 50 | 60 | | |
| | | $V_{DS}$ = 5 V, $I_D$ = 8 A, $T_j$ = 175 °C | | 40 | | |
| **Off Characteristics** | | | | | | |
| Drain Leakage Current | $I_{DSS}$ | $V_R$ = 1700 V, $V_{GS}$ = 0 V, $T_j$ = 25 °C | | 0.2 | 10 | µA |
| | | $V_R$ = 1700 V, $V_{GS}$ = 0 V, $T_j$ = 125 °C | | 0.5 | 50 | |
| | | $V_R$ = 1700 V, $V_{GS}$ = 0 V, $T_j$ = 175 °C | | 2.0 | 100 | |
| Gate Leakage Current | $I_{SG}$ | $V_{SG}$ = 20 V, $T_j$ = 25 °C | | 20 | | nA |

## Electrical Characteristics

| Parameter | Symbol | Conditions | Values min. | Values typ. | Values max. | Unit |
|---|---|---|---|---|---|---|
| **Capacitance Characteristics** | | | | | | |
| Gate-Source Capacitance | $C_{gs}$ | $V_{GS}$ = 0 V, f = 1 MHz | | 830 | | pF |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_D$ = 1 V, f = 1 MHz | | 1070 | | pF |
| Reverse Transfer/Output Capacitance | $C_{rss}/C_{oss}$ | $V_D$ = 1 V, f = 1 MHz | | 240 | | pF |
| **Switching Characteristics** | | | | | | |
| Turn On Delay Time | $t_{d(on)}$ | $T_j$ = 25 ºC, $V_{DS}$ = 1100 V, $I_D$ = 8 A, Two-Level Gate Drive, $R_G$ = 1.5 Ω, $C_G$ = 9 nF, $V_{GH}$ = 20 V, $V_{GL}$ = 6 V, $V_{EE}$ = -5 V, IXDD614 Gate Drive IC, L = 1.05 mH, FWD = GB05SLT12, Refer to Fig. 15 for gate current waveform | | 10 | | ns |
| Rise Time | $t_r$ | | | 10 | | ns |
| Turn Off Delay Time | $t_{d(off)}$ | | | 40 | | ns |
| Fall Time | $t_f$ | | | 50 | | ns |
| Turn-On Energy Per Pulse | $E_{on}$ | | | 375 | | µJ |
| Turn-Off Energy Per Pulse | $E_{off}$ | | | 95 | | µJ |
| Total Switching Energy | $E_{ts}$ | | | 475 | | µJ |
| Turn On Delay Time | $t_{d(on)}$ | $T_j$ = 175 ºC, $V_{DS}$ = 1100 V, $I_D$ = 8 A, Two-Level Gate Drive, $R_G$ = 1.5 Ω, $C_G$ = 9 nF, $V_{GH}$ = 20 V, $V_{GL}$ = 6 V, $V_{EE}$ = -5 V, IXDD614 Gate Drive IC, L = 1.05 mH, FWD = GB05SLT12, Refer to Fig. 15 for gate current waveform | | 10 | | ns |
| Rise Time | $t_r$ | | | 10 | | ns |
| Turn Off Delay Time | $t_{d(off)}$ | | | 55 | | ns |
| Fall Time | $t_f$ | | | 45 | | ns |
| Turn-On Energy Per Pulse | $E_{on}$ | | | 410 | | µJ |
| Turn-Off Energy Per Pulse | $E_{off}$ | | | 85 | | µJ |
| Total Switching Energy | $E_{ts}$ | | | 500 | | µJ |

## Thermal Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| Thermal resistance, junction - case | $R_{thJC}$ | | | 1.03 | | °C/W |

## Figures

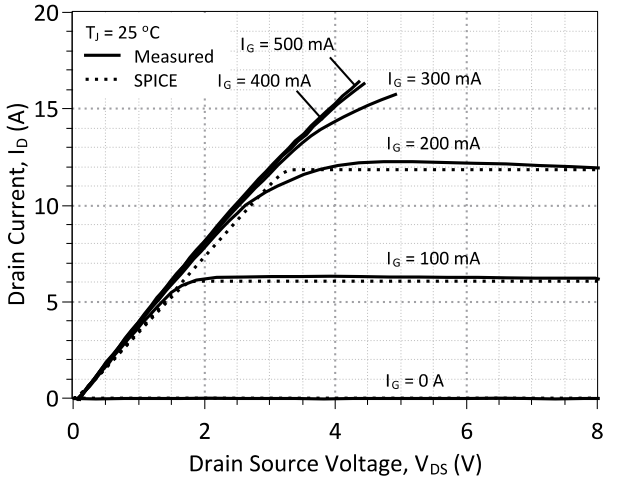



**Figure 1: Typical Output Characteristics at 25 °C**

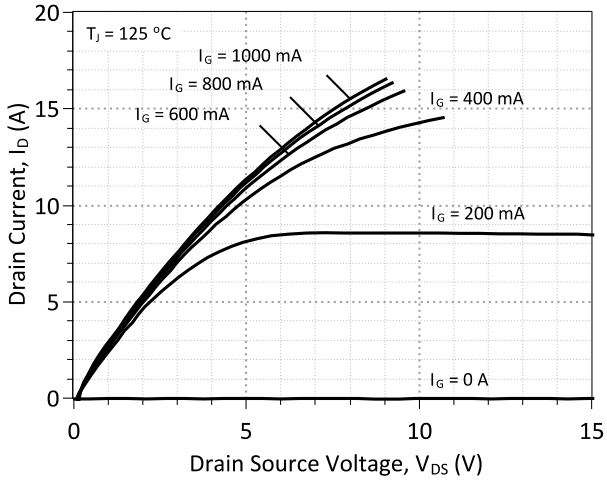



**Figure 2: Typical Output Characteristics at 125 °C**

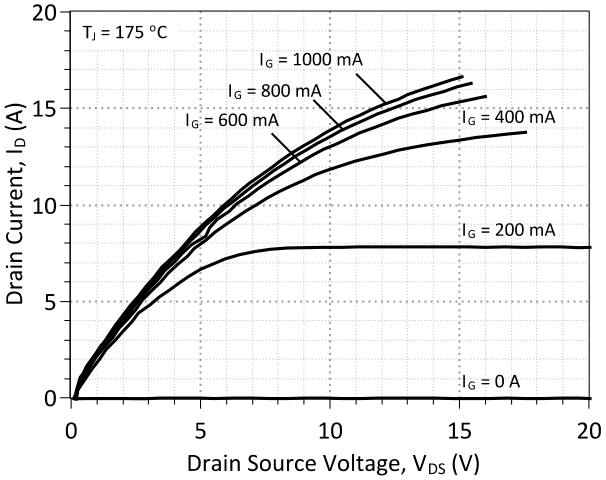



**Figure 3: Typical Output Characteristics at 175 °C**

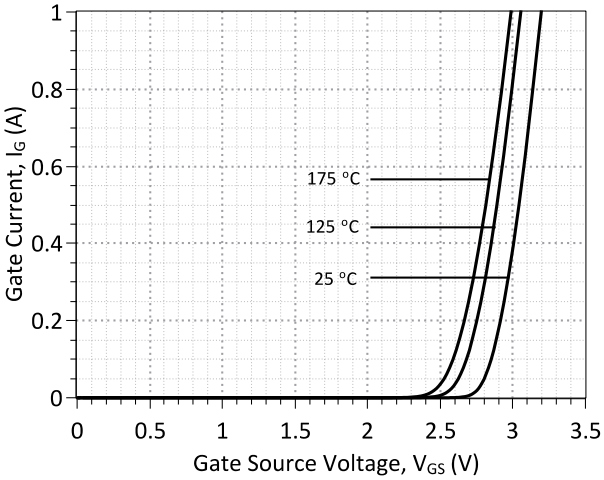



**Figure 4: Typical Gate Source I-V Characteristics vs. Temperature**

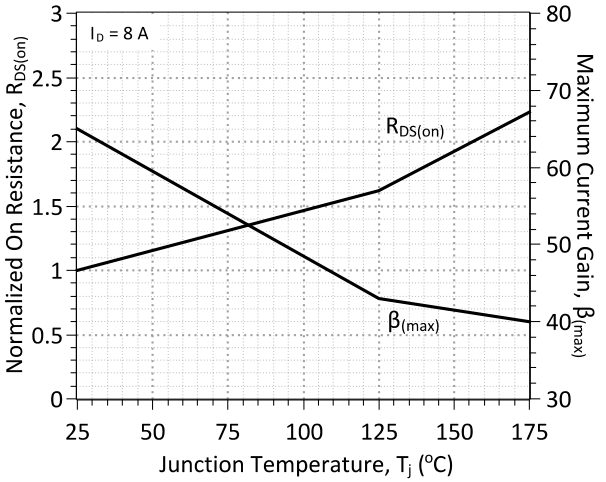



**Figure 5: Normalized On-Resistance and Current Gain vs. Temperature**

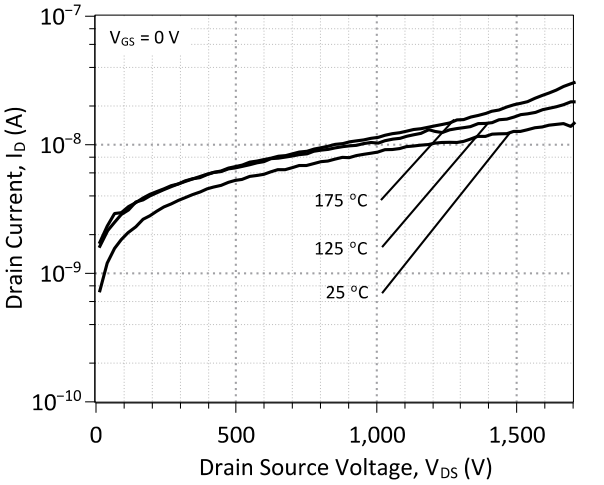



**Figure 6: Typical Blocking Characteristics**

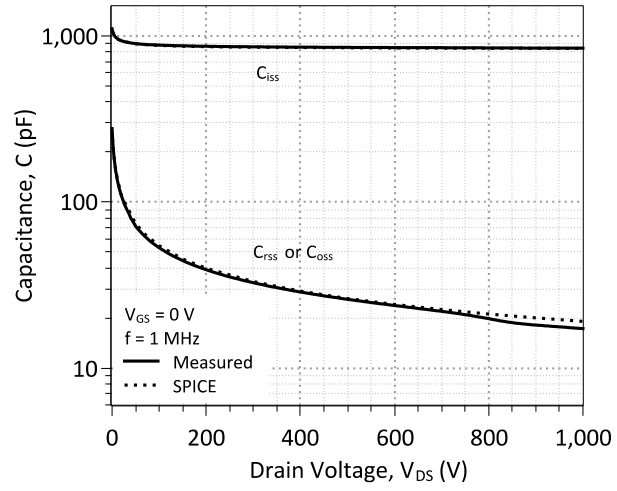



**Figure 7: Capacitance Characteristics**

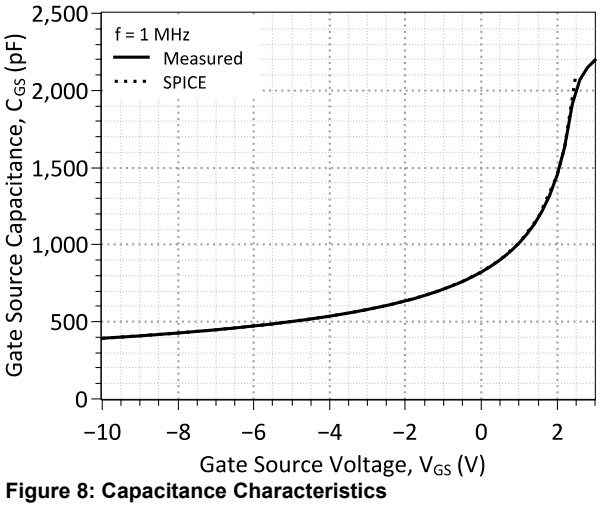



**Figure 8: Capacitance Characteristics**

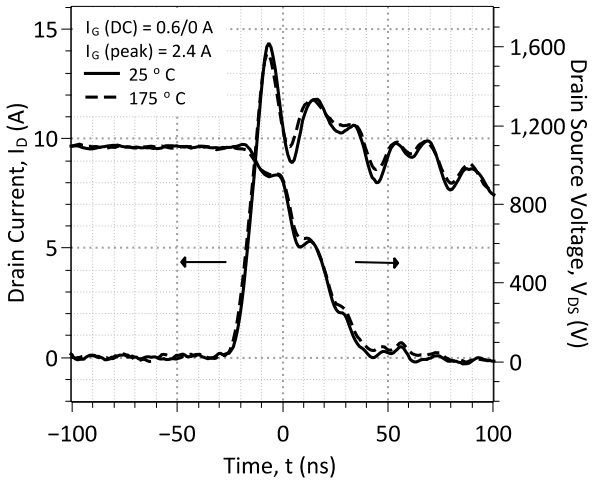



**Figure 9: Typical Hard-switched Turn On Waveforms**

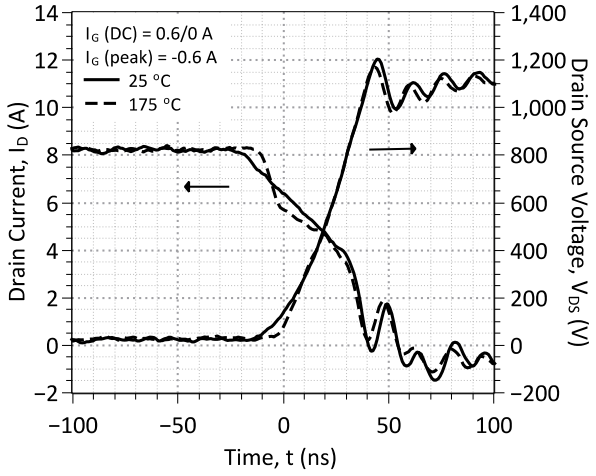



**Figure 10: Typical Hard-switched Turn Off Waveforms**

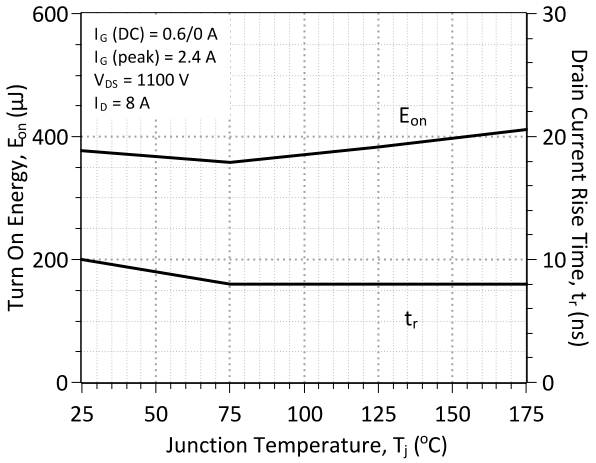



**Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature**

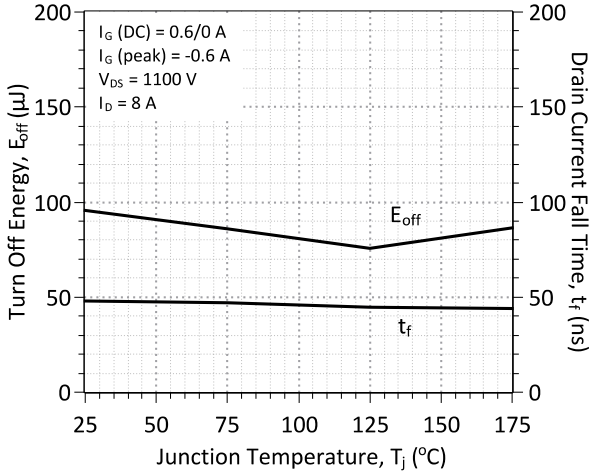



**Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature**

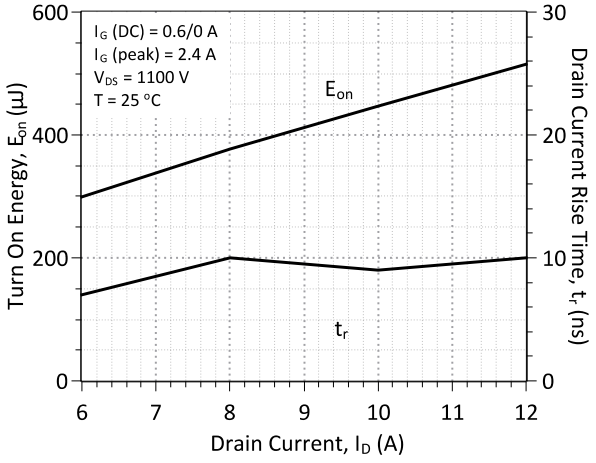



**Figure 13: Typical Turn On Energy Losses vs. Drain Current**

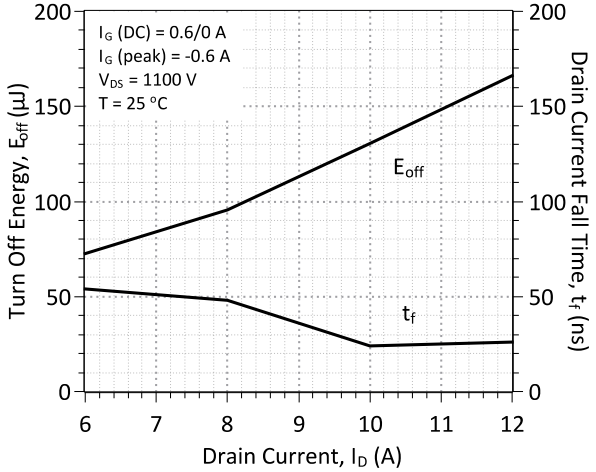



**Figure 14: Typical Turn Off Energy Losses vs. Drain Current**

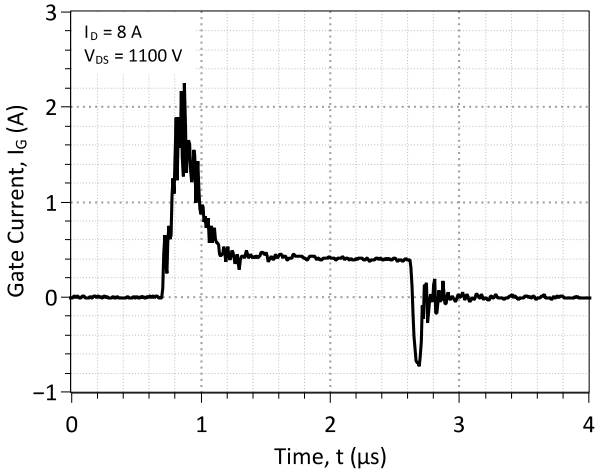



**Figure 15: Typical Gate Current Waveform**

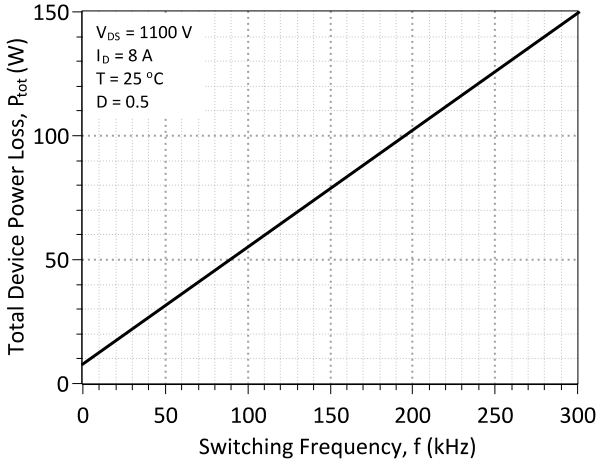



**Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency [1]**

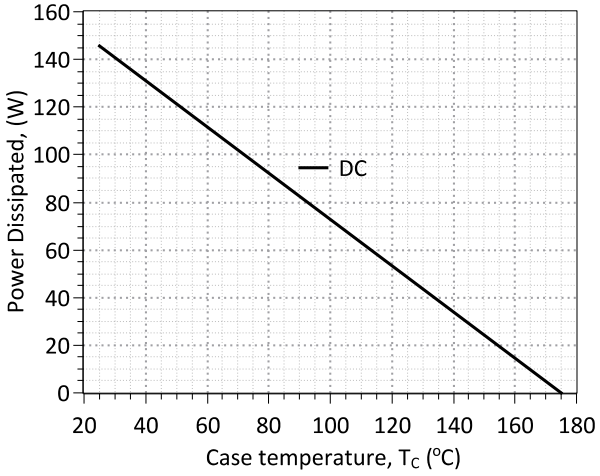



**Figure 17: Power Derating Curve**

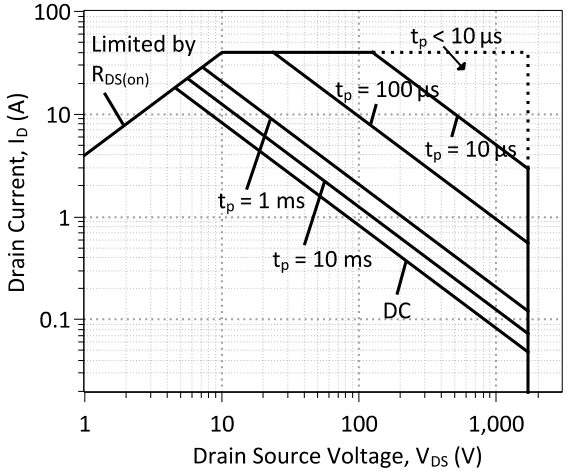



**Figure 18: Forward Bias Safe Operating Area**

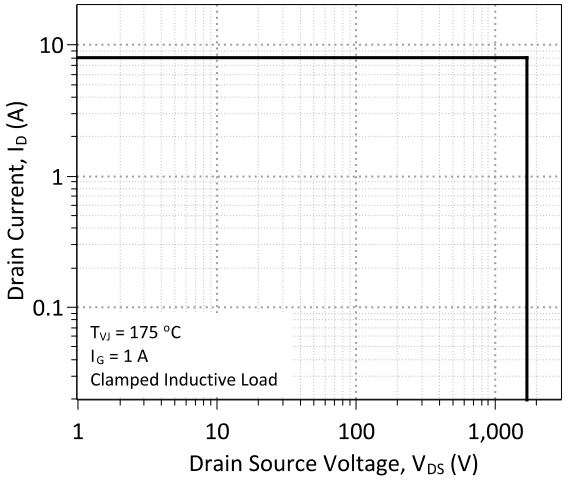



**Figure 19: Turn-Off Safe Operating Area**

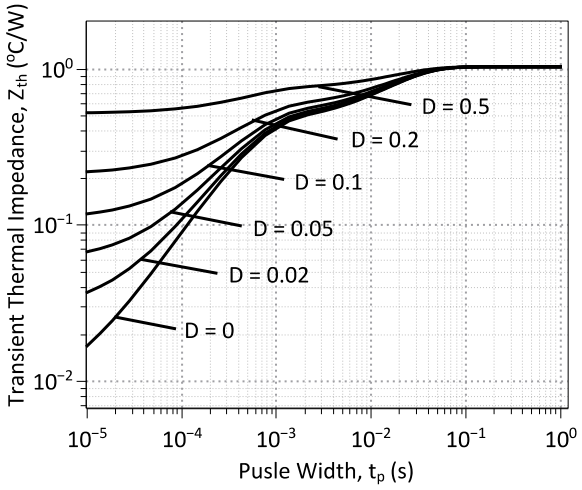



**Figure 20: Transient Thermal Impedance**

[1] – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

## Commercial Gate Drivers Compatible with GA08JT17-247

| Manufacturer | Part Number | Peak Current Capability | Available Features: Peak Current Width Control | Optical Signal Isolation | Desaturation Detection | Under Voltage Lockout |
|---|---|---|---|---|---|---|
| Avago Tech. | ACPL-322J | 2.5 | – | ✓ | ✓ | ✓ |
| IXYS | IXD_604 | 4.0 | – | – | – | – |
| IXYS | IXD_609 | 9.0 | – | – | – | – |
| IXYS | IXD_614 | 14.0 | – | – | – | – |
| Micrel | MIC4452YN | 12.0 | – | – | – | – |
| Microsemi | LX1780QLQ | 15.0 | ✓ | – | – | ✓ |
| Texas Instruments | UCC27322 | 9.0 | – | – | – | – |

SiC SJTs do NOT require a current-driven gate driver. Modern Si IGBT drivers offer sufficient gate currents to drive SJTs. This is a partial list of widely available commercial Silicon IGBT/MOSFET gate drivers which may be used to drive the GA08JT17-247. Specific product information including advanced features and pinouts should be obtained from the individual product manufacturer's websites.

The GA08JT17-247 can be driven similar to silicon IGBTs or MOSFETs in which a gate driver IC is used to supply positive gate current peaks to the device at turn-on and negative current peaks at turn-off. Unlike the IGBT or MOSFET, the GA08JT17-247 also requires a continuous gate current for the device to remain on after the initial current peak. An example gate current waveform for the GA08JT17-247 is shown in Fig. 15.

## Single-Level SJT Gate Drive

Producing the necessary gate current peaks and continuous currents can be accomplished by using a gate drive circuit shown in Fig. 21. The gate driver output node is connected to an NPN/PNP silicon BJT pair in a totem pole configuration which provide gate current to the SJT gate. The NPN/PNP pair are controlled by the gate drive IC connected through base resistor $R_b$. The pair's output at node $N_1$ is connected to gate resistor $R_G$ and capacitor $C_G$ placed in parallel and connected to the SJT gate terminal. The gate resistor determines the continuous gate current. The gate capacitor produces positive and negative current peaks, which enable fast charging and discharging of the SJT's terminal capacitances. Additional detail on the single-level SJT gate driving technique is discussed in GeneSiC Semiconductor Application Note AN-10A. (http://www.genesicsemi.com/index.php/references/notes)

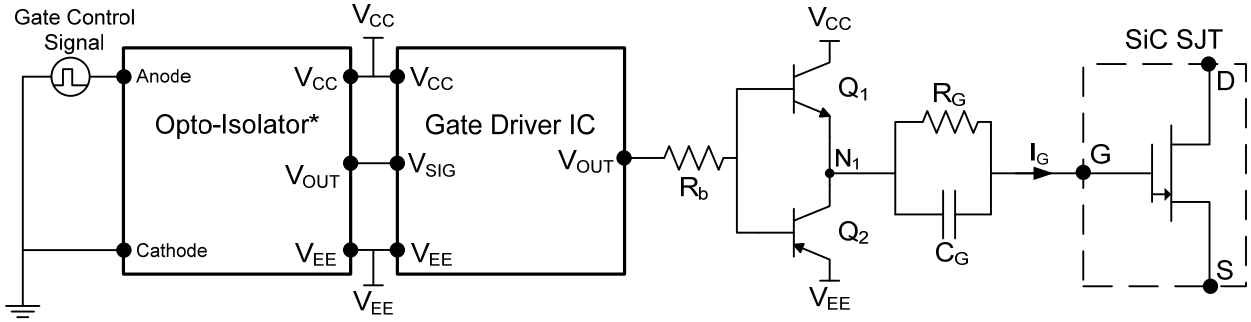



**Figure 21: Single-Level SJT Gate Diver Configuration (* External signal isolation is recommended for non-isolated gate driver ICs.)**

## Single-Level Gate Drive Conditions

| Parameter | Symbol | Conditions | Values: Min. | Optimum | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | | 15 | 20 | V |
| Negative Supply Voltage | $V_{EE}$ | | -10 | -5 | | V |
| Output Current, Peak | $I_{OUT,\ pk}$ | Package Limited, | 1.0 | 2.0 | | A |
| Output Current, Continuous | $I_{OUT}$ | $I_D$ = 8.0 A, T = 175 °C | 0.3 | 0.5 | | A |
| **Output Gate Components** | | | | | | |
| Gate Resistance | $R_G$ | $V_{CC}$ = 15 V, $I_G$ ≈ 0.5 A, T = 175 °C | 15 | 22 | | Ω |
| Gate Capacitance | $C_G$ | $V_{CC}$ = 15 V $I_{G,pk}$ ≈ 1.5 A, T = 175 °C | 5 | 9 | | nF |
| Base Resistor | $R_b$ | | | 10 | | Ω |
| NPN/PNP BJT Output Buffer | $Q_1$, $Q_2$ | 2N6107/2N6292 pair or equivalent ** | | | | |

** - Complimentary BJT pair with $I_C$ ≥ 5 A and $V_{CEO}$ ≥ 60 V

## Two-Level SJT Gate Drive

The GA08JT17-247 can also be driven with a gate drive circuit shown in Fig. 22, in which two gate drive ICs and NPN/PNP pairs are operated with different supply voltage ($V_{CC}$) levels in order to minimize gate drive losses. By using a separate lower voltage output gate driver IC connected to gate resistor $R_G$, the power consumption of the continuous current is reduced. Additional detail on the two-level SJT gate driving technique is discussed in GeneSiC Semiconductor Application Note AN-10B. (http://www.genesicsemi.com/index.php/references/notes)

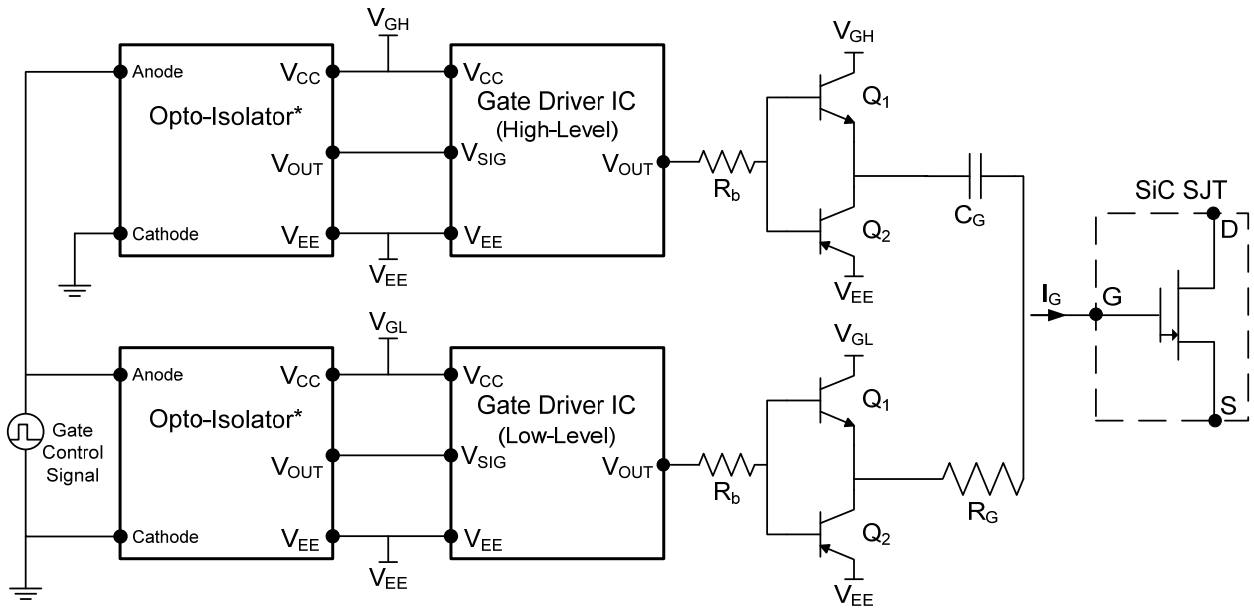



**Figure 22: Two-Level SJT Gate Diver Configuration for Reduced Drive Losses (* External signal isolation is recommended for non-isolated gate driver ICs.)**

## Two-Level Gate Drive Conditions

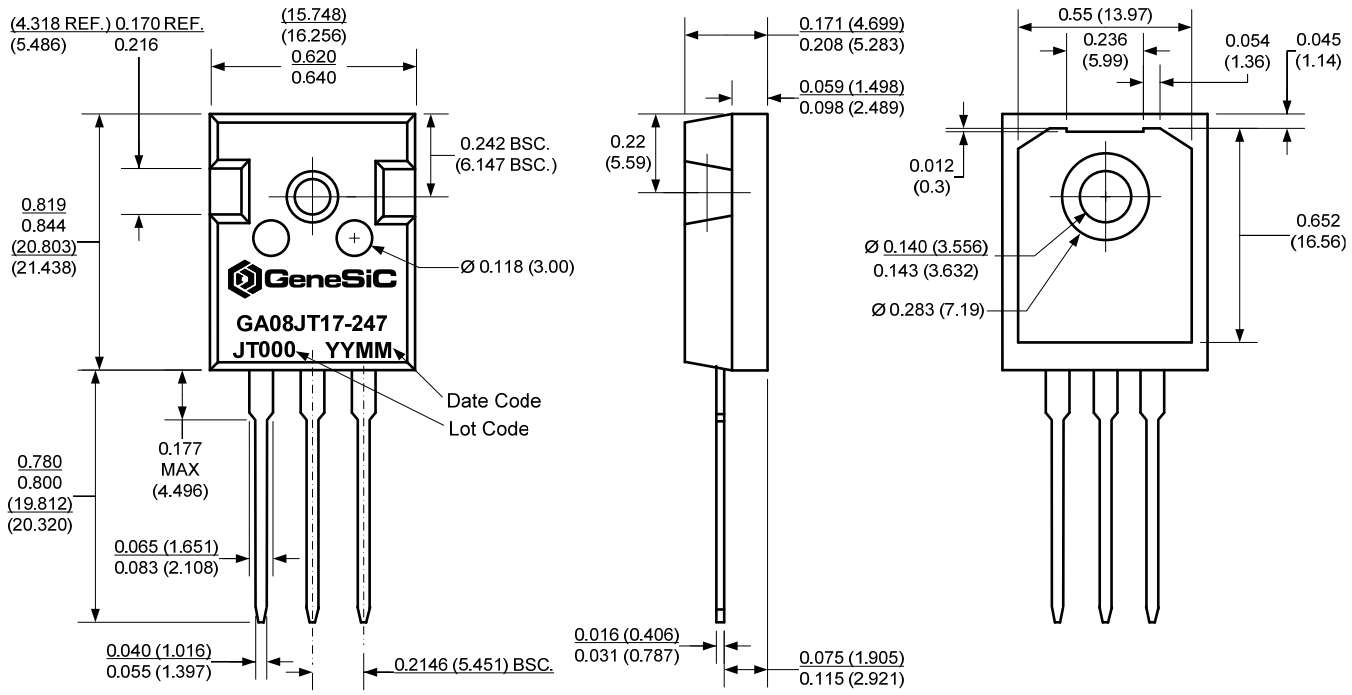
| Parameter | Symbol | Conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | min. | Optimum | max. | |
| Supply Voltage, High Level Driver | $V_{CC}$ ($V_{GH}$+) | | 15 | 19 | | V |
| Supply Voltage, Low Level Driver | $V_{CC}$($V_{GL}$+) | | 5 | 6 | | V |
| Negative Supply Voltage | $V_{EE}$ | | -10 | -5 | | V |
| Output Current, Peak | $I_{OUT}$ | Package Limited, | 1.0 | 2.0 | | A |
| Output Current, Continuous | $I_{OUT}$ | $I_D$ = 8.0 A, T = 175 °C | 0.3 | 0.5 | | A |
| **Output Gate Components** | | | | | | |
| Gate Resistance | $R_G$ | $V_{GL}$ = 6.0 V, $I_G$ ≈ 0.5 A, T = 175 °C | | 1.6 | 5 | Ω |
| Gate Capacitance | $C_G$ | $V_{GH}$ = 20 V, $I_{G,pk}$ ≈ 1.5 A, T = 175 °C | 5 | 9 | | nF |
| Base Resistor | $R_b$ | | | 10 | | Ω |
| NPN/PNP BJT Output Buffer | $Q_1$, $Q_2$ | 2N6107/2N6292 pair or equivalent** | | | | |

** - Complimentary BJT pair with $I_C$ ≥ 5 A and $V_{CEO}$ ≥ 60 V

+ – Consult application note AN-10B for more information on parameters $V_{GH}$ and $V_{GL}$.

## Package Dimensions:

**TO-247AB** **PACKAGE OUTLINE**




**NOTE**
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

| Revision History | | | |
|---|---|---|---|
| Date | Revision | Comments | Supersedes |
| 2014/02/06 | 6 | Updated Electrical Characteristics | |
| 2013/12/18 | 5 | Updated Gate Drive Section | |
| 2013/11/12 | 4 | Updated Electrical Characteristics | |
| 2013/08/27 | 3 | Updated Switching Characteristics | |
| 2013/06/24 | 2 | Updated Electrical Characteristics | |
| 2013/02/21 | 1 | Switching Data Added | |
| 2012/12/03 | 0 | Initial release | |

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## SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/products_sic/sjt/GA08JT17-247_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA08JT17-247.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   1.0           $
*     $Date:   26-AUG-2013       $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
*     COPYRIGHT (C) 2013 GeneSiC Semiconductor Inc.
*     ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model GA08JT17 NPN
+ IS       3.73E-47
+ ISE      5.50E-27
+ EG       3.2
+ BF       63
+ BR       0.55
+ IKF      200
+ NF       1
+ NE       2.021
+ RB       0.26
+ RE       0.103394007
+ RC       0.151605993
+ CJC      2.77E-10
+ VJC      3.023103628
+ MJC      0.460762158
+ CJE      8.23E-10
+ VJE      2.945448229
+ MJE      0.498044294
+ XTI      3
+ XTB      -0.7
+ TRC1     7.50E-3
+ VCEO     1700
+ ICRATING 8
+ MFG      GeneSiC_Semiconductor
*
* End of GA08JT17 SPICE Model
```