TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (Ultra-High-Speed U-MOSⅢ)

# **TK50X15J1**

#### **DC-DC Converters**

• Low drain-source ON-resistance:  $R_{DS (ON)} = 22 \text{ m}\Omega \text{ (typ.)}$ 

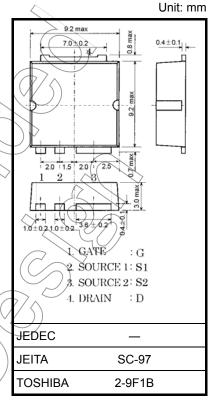
• High forward transfer admittance: |Yfs| = 90 S (typ.)

• Low leakage current:  $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 150 \text{ V)}$ 

• Enhancement mode:  $V_{th}$  = 2.0 to 4.0 V ( $V_{DS}$  = 10 V,  $I_D$  = 1 mA)

### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics		Symbol	Rating	Unit
Drain-source voltage		$V_{DSS}$	150	(V)
Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )		$V_{DGR}$	150	$(\sqrt{y})$
Gate-source voltage		$V_{GSS}$	±20	A
Drain current	DC (Note 1)	ID	50	A
	Pulse (Note 1)	I <sub>DP</sub>	150	$\supset$ $\cap$
Drain power dissipation (Tc = 25°C)		$P_{D}$	125	W
Single pulse avalanche energy (Note 2)		EAS	182	mJ
Avalanche current		I <sub>AR</sub>	50	<b>(</b> A
Repetitive avalanche energy (Note 3)		EAR	10.9	mJ
Channel temperature (Note 4)		Tch	175	°C
Storage temperature range (Note 4)		(T <sub>stg</sub>	-55 to 175	\\°C



Weight: 0.74 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

### Thermal Characteristics

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Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	Rth (ch-c)	1.2	°C/W

Note 1: Ensure that the channel temperature does not exceed 175°C.

Note 2:  $V_{DD} = 50V$ ,  $T_{ch} = 25^{\circ}C$  (initial),  $L = 110~\mu H$ ,  $R_G = 25~\Omega$ ,  $I_{AR} = 50A$ 

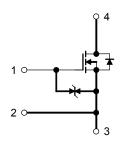
Note 3: Repetitive rating: pulse width limited by maximum channel temperature

Note 4: The definitions of the absolute maximum channel and storage temperatures are base on AEC-Q101.

This transistor is an electrostatic-sensitive device. Handle with care.

## **Circuit Configuration**

Note: Use the S1 pin to return the gate signal to source. Board traces should be designed so the main current flows to the S2 pin.



## Electrical Characteristics (Note 5) (Ta = 25°C)

Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage cur	rent	I <sub>GSS</sub>	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±10	μА
Drain cut-OFF cu	ırrent	I <sub>DSS</sub>	V <sub>DS</sub> = 150 V, V <sub>GS</sub> = 0 V	_	_	10	μΑ
Drain-source breakdown voltage		V (BR) DSS	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	150	_	_	V
		V (BR) DSX	$I_D = 10$ mA, $V_{GS} = -20$ V	95	_	_	V
Gate threshold vo	oltage	V <sub>th</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.0	) >_	4.0	V
Drain-source ON	-resistance	R <sub>DS</sub> (ON)	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 25 A	<u> </u>	22	30	mΩ
Forward transfer	admittance	Y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 25 A	45	90	_	S
Input capacitance	9	C <sub>iss</sub>			4300	_	
Reverse transfer capacitance		C <sub>rss</sub>	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	<sup>2</sup> —	210	_	pF
Output capacitance		C <sub>oss</sub>		_	640	_	
Switching time	Rise time	t <sub>r</sub>	V <sub>GS</sub> I <sub>D</sub> =25 A V <sub>OUT</sub>	- (	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	<u></u>	
	Turn-ON time	t <sub>on</sub>	0 V	_((	30	) —	
	Fall time	t <sub>f</sub>	4 × × × × × × × × × × × × × × × × × × ×		15	_	ns
	Turn-OFF time	t <sub>off</sub>	Duty $\leq$ 1%, $t_{W} = 10 \mu s$		85	_	
Total gate charge (gate-source plus		Q <sub>g</sub>		) _	75	_	
Gate-source charge1		Q <sub>gs1</sub>	V <sub>DD</sub> ≈ 120 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		25	_	nC
Gate-drain ("miller") charge		Q <sub>gd</sub>		_	25	_	
Gate switch charge		Q <sub>SW</sub>		_	33	_	

Note 5: The S1 and S2 pins should be grounded together, except when measuring the switching time.

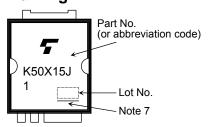
## Source-Drain Ratings and Characteristics (Note 6) (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1, Note 6)	IDR	,	_	_	50	Α
Pulse drain reverse current (Note 1,Note 6)	1 <sub>DRP</sub> 1	_	_	_	150	Α
Continuous drain reverse current (Note 1, Note 6)	I <sub>DR</sub> 2	_	_	_	1	Α
Pulse drain reverse current (Note 1,Note 6)	I <sub>DRP</sub> 2	_	_	_	4	Α
Forward voltage (diode)	V <sub>DS2F</sub>	I <sub>DR</sub> 1 = 50 A, V <sub>GS</sub> = 0 V	_	_	-1.5	V
Reverse recovery time	t <sub>rr</sub>	I <sub>DR</sub> = 50 A, V <sub>GS</sub> = 0 V,	_	95	_	ns
Reverse recovery charge	Q <sub>rr</sub>	dl <sub>DR</sub> /dt = 100 A/μs	_	450	_	nC

Note 6: \(\lambda\_{DR}\)1, \(\lambda\_{DRP}\)1: Current flowing between the drain and S2 pins. Ensure that the S1 pin is left open. \(\lambda\_{DR}\)2, \(\lambda\_{DRP}\)2: Current flowing between the drain and S1 pins. Ensure that the S2 pin is left open. The S1 and S2 pins should be grounded together, unless otherwise noted.

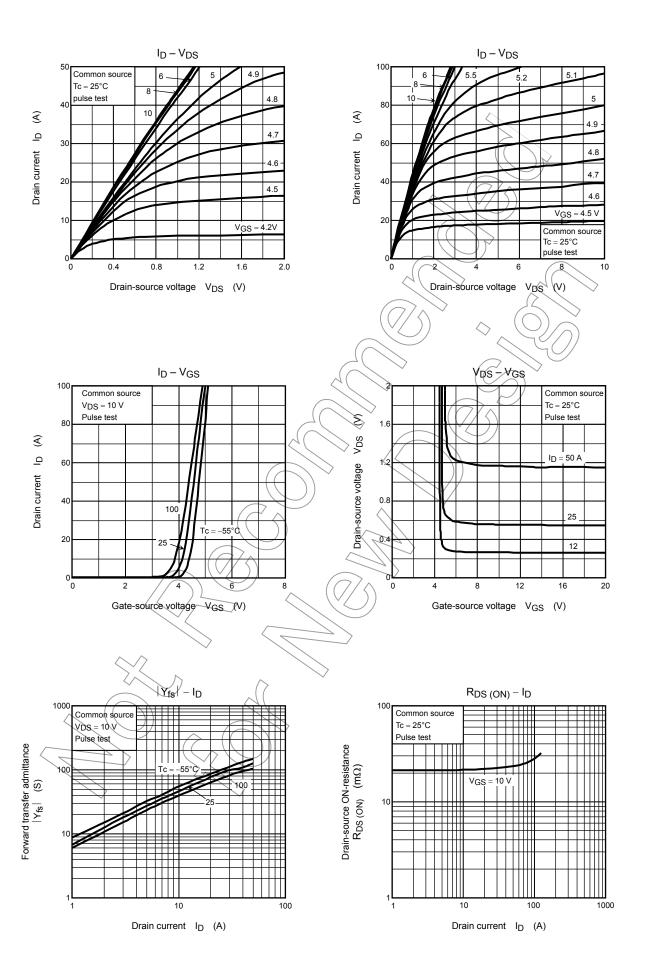
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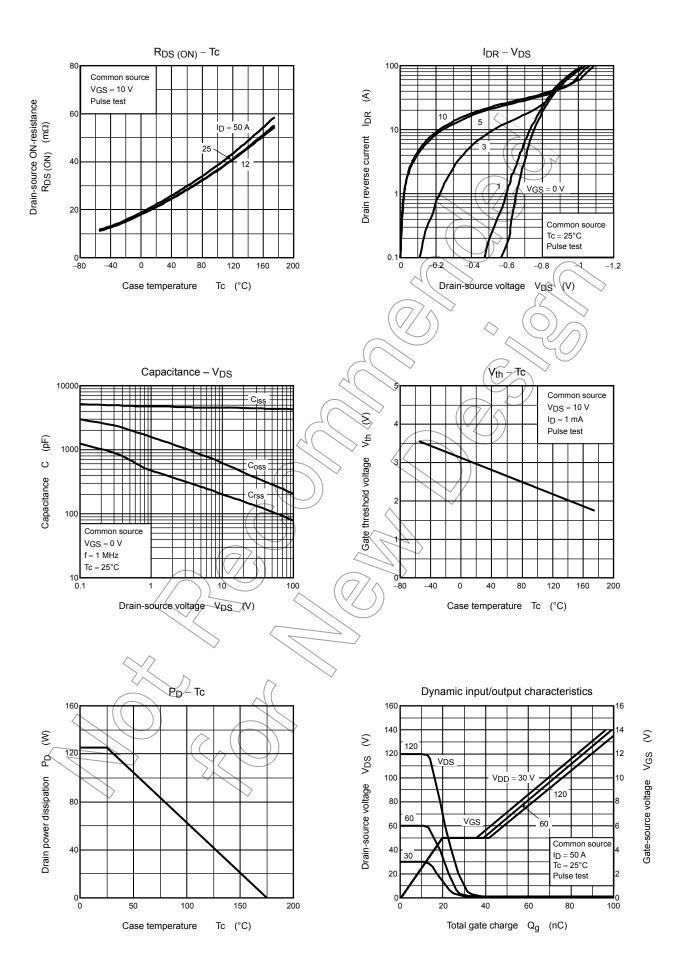
#### **Marking**

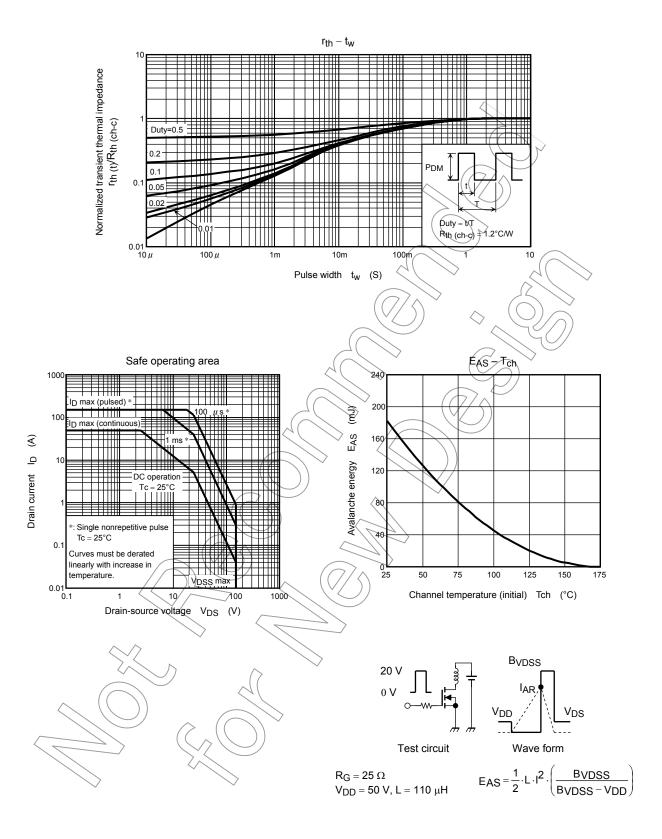


Note 7: A line under a Lot No. identifies the indication of product Labels. [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

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