STANSON

STN1304 Lead-free

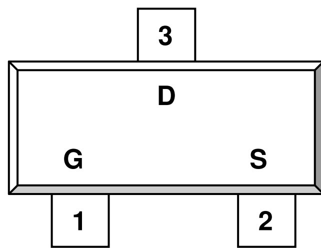
N Channel Enhancement Mode MOSFET

2.0A

DESCRIPTION

STN1304 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology.This high density process is especially tailored to minimize on-state resistance.These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management, other battery powered circuits, and low in-line power loss are required. The product is in a very small outline surface mount package.

PIN CONFIGURATION
SOT-323

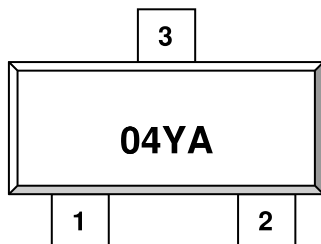


1.Gate 2.Source 3.Drain

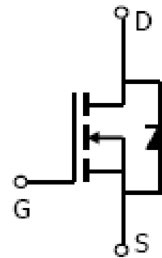
FEATURE

- 20V/2.0A, $R_{DS(ON)}$ = 225mΩ @VGS = 4.5V
- 20V/1.5A, $R_{DS(ON)}$ = 315mΩ @VGS = 2.5V
- 20V/1.0A, $R_{DS(ON)}$ = 425mΩ @VGS = 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-323 package design

PART MARKING
SOT-323



Y: Year Code A: Process Code



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120 Bentley Square, Mountain View, Ca 94040 USA
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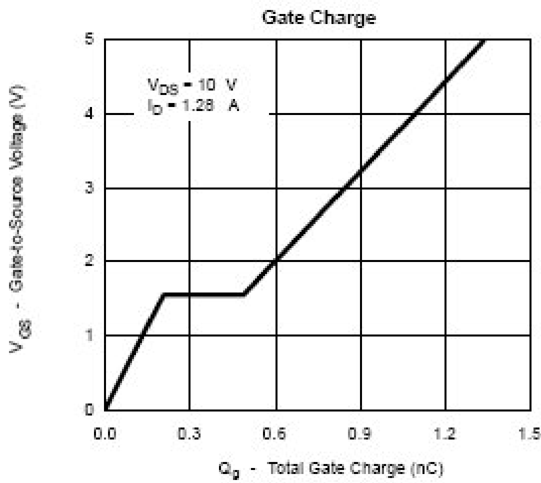
ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

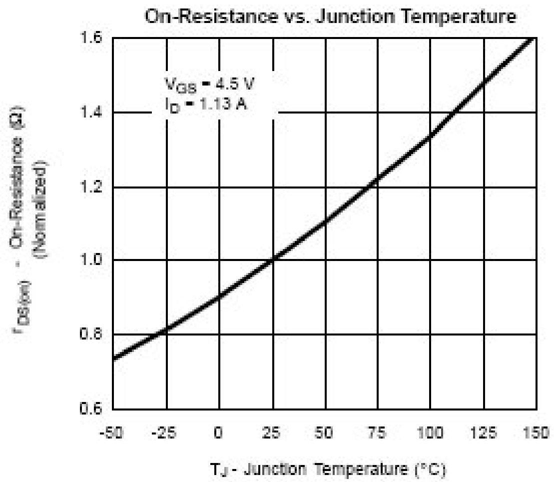
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±12	V
Continuous Drain CurrentTJ=150℃)	T_A=25℃ T_A=70℃	I_D	2.0 1.5	A
Pulsed Drain Current		I_{DM}	10	A
Continuous Source Current (Diode Conduction)		I_S	1.6	A
Power Dissipation	T_A=25℃ T_A=70℃	P_D	1.25 0.8	W
Operation Junction Temperature		T_J	150	℃
Storgae Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	105	℃/W

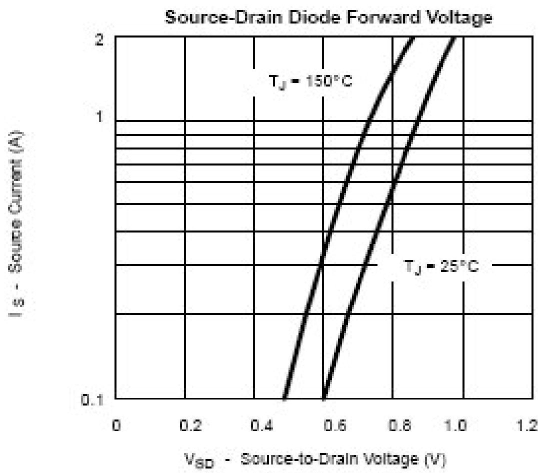
ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

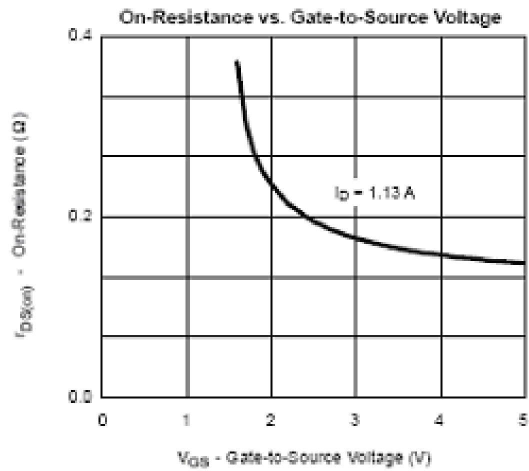
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250uA$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=VGS, I_D=250uA$	0.35		1.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=55$℃			5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=2.0A$ $V_{GS}=2.5V, I_D=1.5A$ $V_{GS}=1.8V, I_D=1.0A$		0.150 0.210 0.320	0.225 0.315 0.425	Ω
Forward Transconductance	g_{fs}	$V_{DS}=10V, I_D=1.2A$		10		S
Diode Forward Voltage	V_{SD}	$I_S=0.5A, V_{GS}=0V$		0.80	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V$ $V_{GS}=4.5V$ $I_D=0.7A$		1.2	1.5	nC
Gate-Source Charge	Q_{gs}			0.2		
Gate-Drain Charge	Q_{gd}			0.3		
Input Capacitance	C_{iss}	$V_{DS}=10V$ $V_{GS}=0V$ F=1MHz		110		pF
Output Capacitance	C_{oss}			34		
Reverse Transfer Capacitance	C_{rss}			16		
Turn-On Time	$t_{d(on)}$	$V_{DD}=10V$ $R_L=10\Omega$ $I_D=1.0A$ $V_{GEN}=4.5V$ $R_G=6\Omega$		5	10	nS
	t_r			8	15	
Turn-Off Time	$t_{d(off)}$			10	18	
	t_f			1.2	2.8	

TYPICAL CHARACTERICTICS (25℃ Unless noted)









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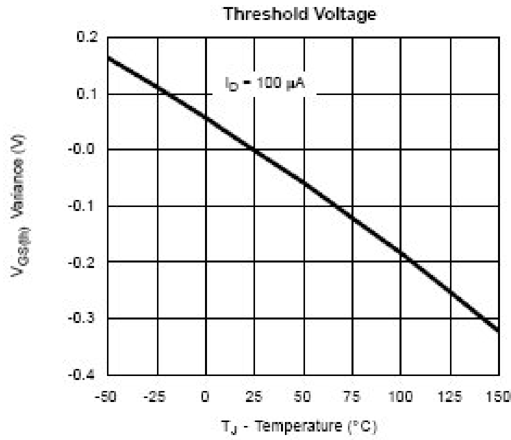

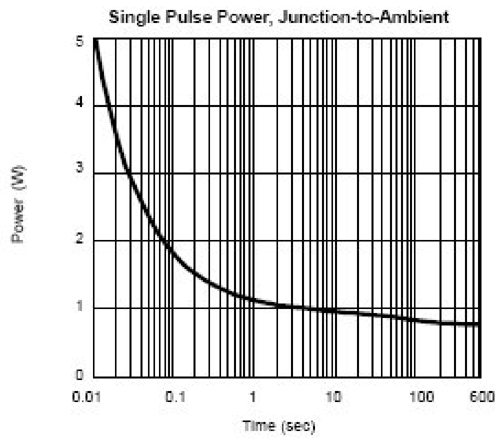

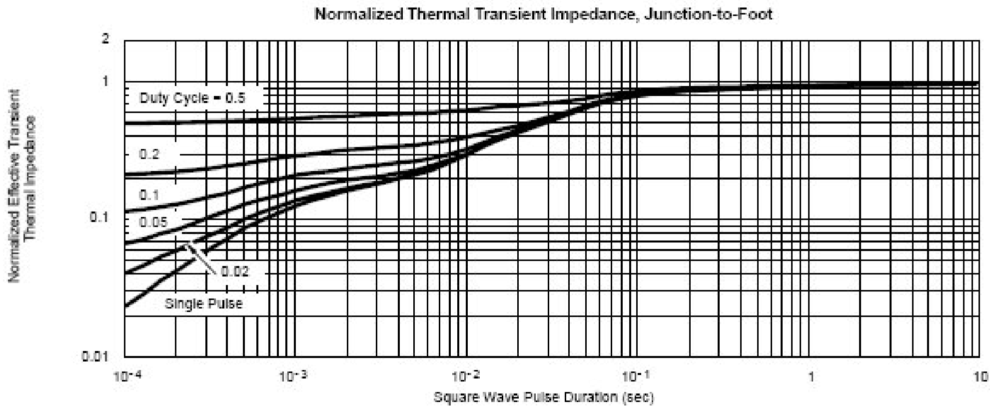

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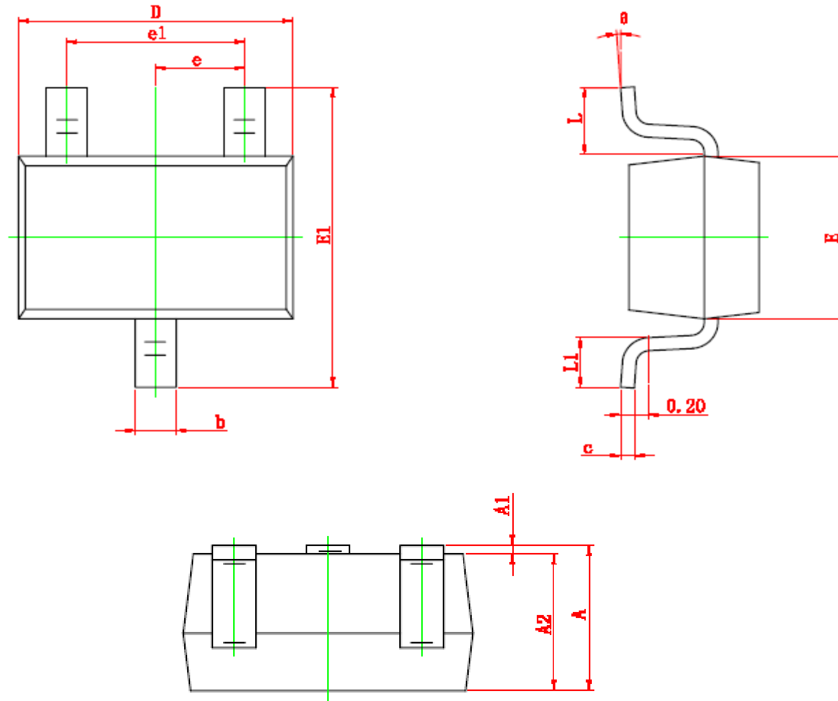
SOT-323 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.200	0.400	0.008	0.016
c	0.080	0.150	0.003	0.006
D	2.000	2.200	0.079	0.087
E	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650 TYP		0.026 TYP	
e1	1.200	1.400	0.047	0.055
L	0.525 REF		0.021 REF	
L1	0.260	0.460	0.010	0.018
θ	0°	8°	0°	8°