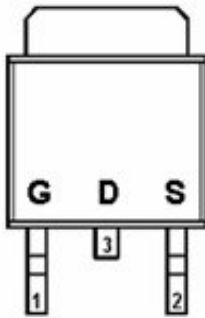


**DESCRIPTION**

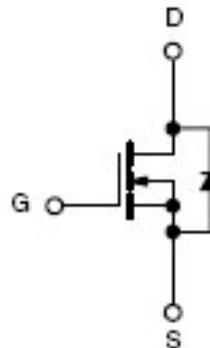
STN18D20 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

**PIN CONFIGURATION  
TO-252**

**PART MARKING**


**Y: Year Code**  
**A: Date Code**  
**Q: Process Code**

**FEATURE**

- 200V/12A,  $R_{DS(ON)} = 170m\Omega$ (Typ.) @  $V_{GS} = 10V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252 package design



**STN18D20**

N Channel Enhancement Mode MOSFET

18.0A

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	200	V
Gate-Source Voltage	VGSS	±30	V
Continuous Drain Current (TJ=150°C)	ID	18 11.4	A
		TA=25°C TA=100°C	
Pulsed Drain Current	IDM	36	A
Avalanche Current	IAS	17	mJ
Power Dissipation	PD	112	W
		TA=25°C	
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	80	°C/W



**STN18D20**

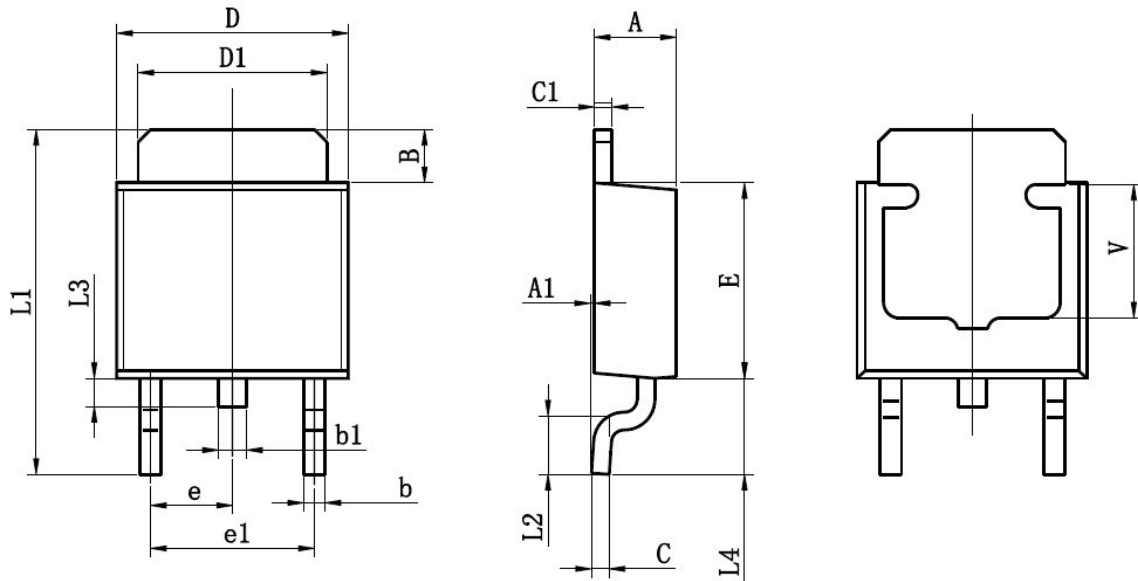


N Channel Enhancement Mode MOSFET

18.0A

**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	200			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2		5	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 30V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=160V, V_{GS}=0V$			2	$\mu A$
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	18			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$		170	220	m $\Omega$
Forward Transconductance	gfs	$V_{DS}=15V, I_D=20A$		8.5		S
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$			1	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=160V, V_{GS}=10V$ $I_D=12 A$		17.6	25	nC
Gate-Source Charge	$Q_{gs}$			7.6	11	
Gate-Drain Charge	$Q_{gd}$			3.7	5.2	
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS}=0V$ $f=1MHz$		1000	1400	pF
Output Capacitance	$C_{oss}$			110	155	
Reverse Transfer Capacitance	$C_{rss}$			2.4	3.5	
Turn-On Time	$t_{d(on)}$ $t_r$	$V_{DS}=100, R_G=3.3$ $V_{GEN}=10V, I_D=12 A$ $R_G=1.0\Omega$		9.4	19	nS
Turn-Off Time	$t_{d(off)}$ $t_f$			23	41	
				18.4	37	
				15.6	21.8	

**PACKAGE OUTLINE SOP-8P**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	