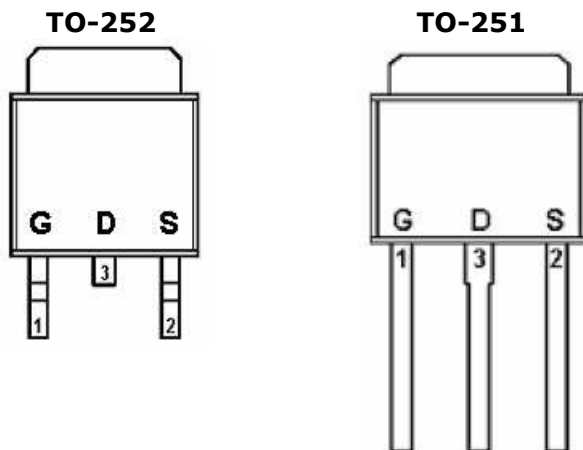
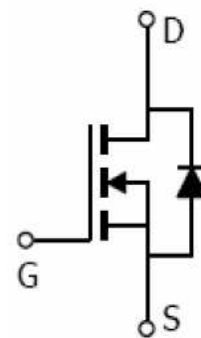
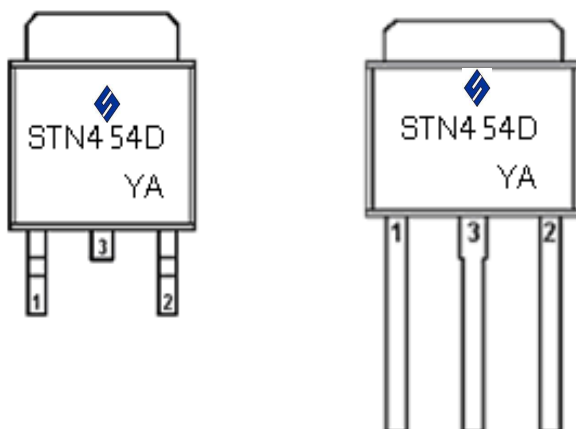


DESCRIPTION

STN454D is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. The STN454D has been designed specially to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

PIN CONFIGURATION (D-PAK)

FEATURE

- 40V/12.0A, $R_{DS(ON)} = 25m\Omega$ (Typ.) @ $V_{GS} = 10V$
- 40V/6.0A, $R_{DS(ON)} = 27m\Omega$ @ $V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252, TO-251 package design

PART MARKING


Y: Year Code A: Process Code



STN454D



N Channel Enhancement Mode MOSFET

10.0A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	40	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	TA=25°C 12.0	A
		TA=70°C 10.0	
Pulsed Drain Current	IDM	30	A
Continuous Source Current (Diode Conduction)	IS	12	A
Power Dissipation	PD	TA=25°C 50	W
		TA=70°C 25	
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	60	°C/W



STN454D



N Channel Enhancement Mode MOSFET

10.0A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=10mA$	40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V$			1	uA
		$V_{DS}=32V, V_{GS}=0V$ $T_J=85^\circ C$			5	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=12A$ $V_{GS}=4.5V, I_D=6A$		25 27		mΩ
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=12A$		25		S
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$			1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=10V, V_{DS}=20$ $I_D=12A$		11		nC
Gate-Source Charge	Q_{gs}			4.8		
Gate-Drain Charge	Q_{gd}			1.8		
Input Capacitance	C_{iss}	$V_{DS} = 20V, V_{GS}=0V$ $F=1MHz$		850		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			75		
Turn-On Time	$t_{d(on)}$	$V_{DD}=20V, R_L= 4\Omega$ $I_D=5.0A, V_{GEN}=10V$ $R_G=1\Omega$		6	12	nS
	t_r			10	20	
Turn-Off Time	$t_{d(off)}$			20	36	
	t_f			6	12	

TYPICAL CHARACTERISTICS

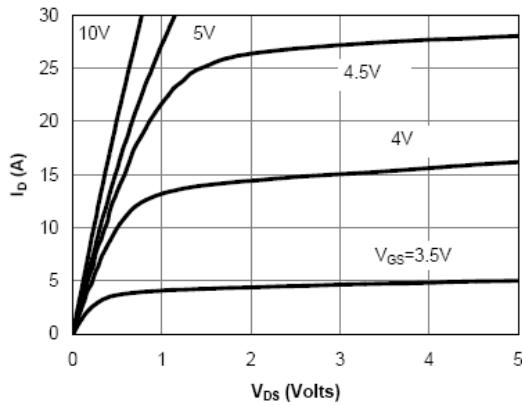


Fig 1: On-Region Characteristics

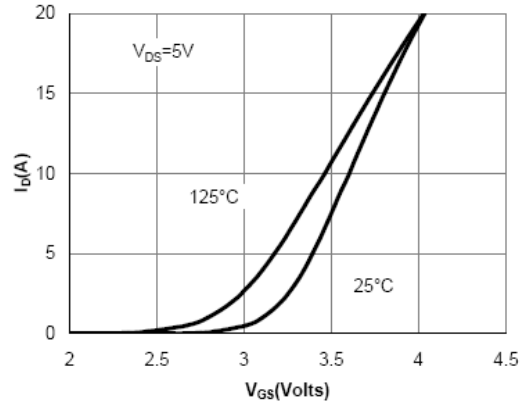


Figure 2: Transfer Characteristics

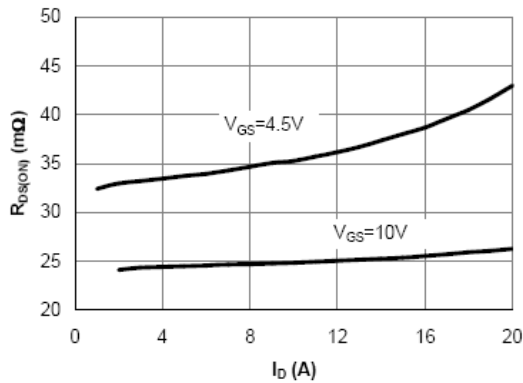


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

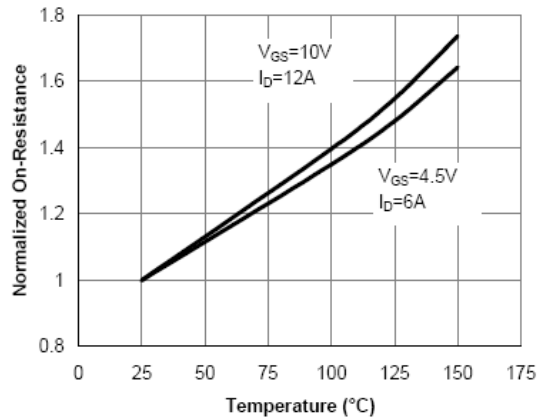


Figure 4: On-Resistance vs. Junction Temperature

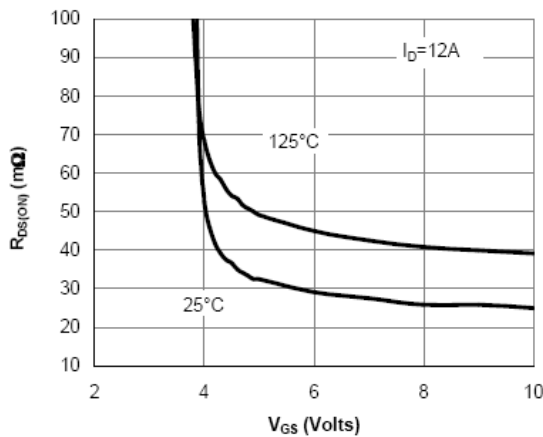


Figure 5: On-Resistance vs. Gate-Source Voltage

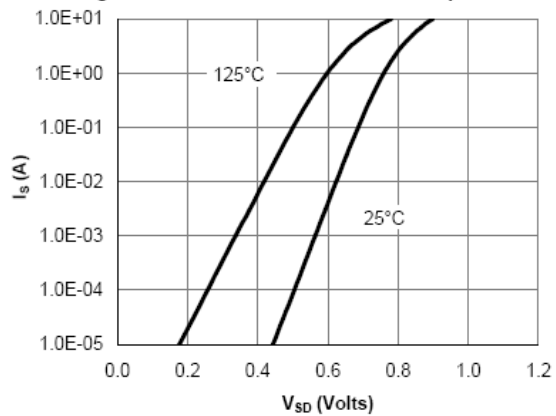


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS

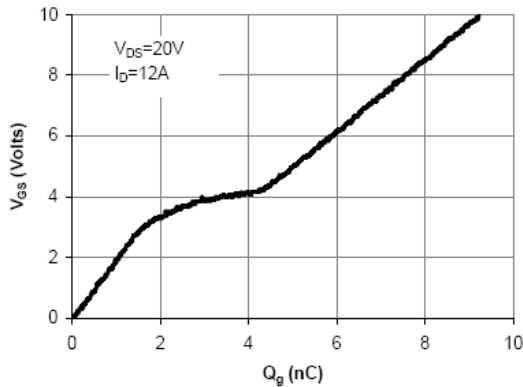


Figure 7: Gate-Charge Characteristics

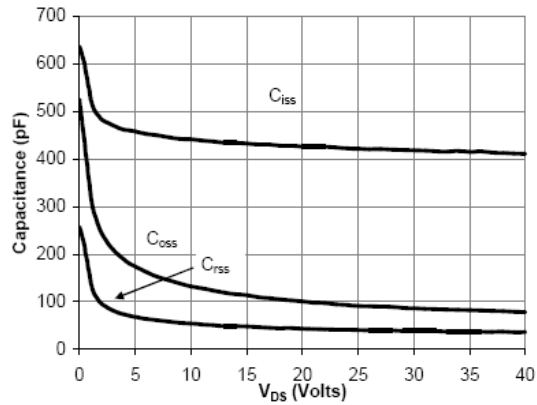


Figure 8: Capacitance Characteristics

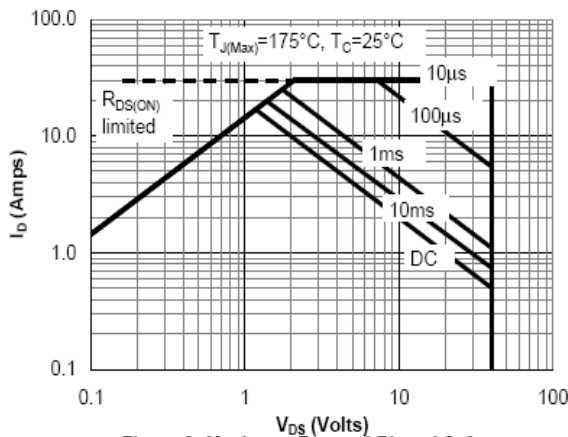


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

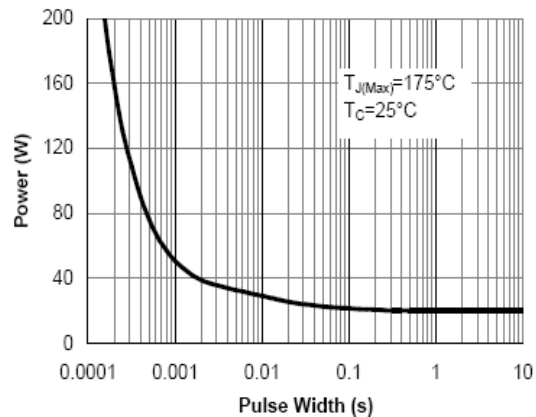


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

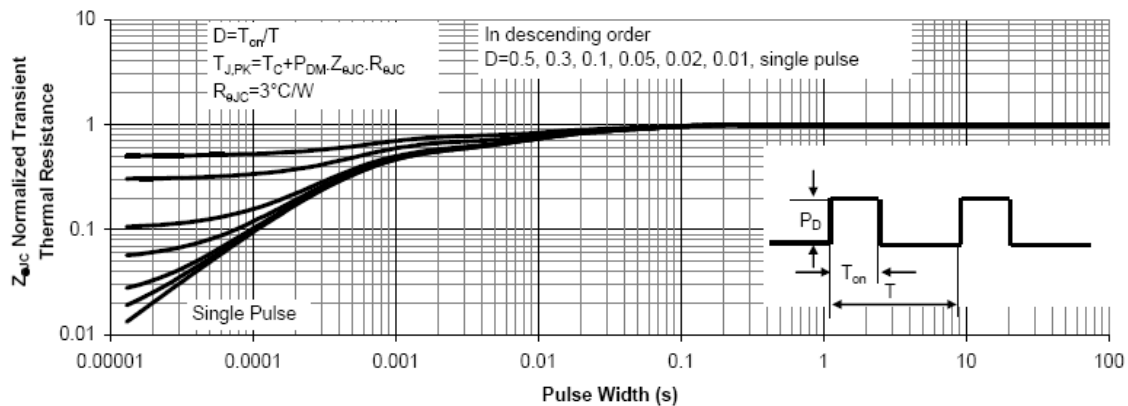


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL CHARACTERISTICS

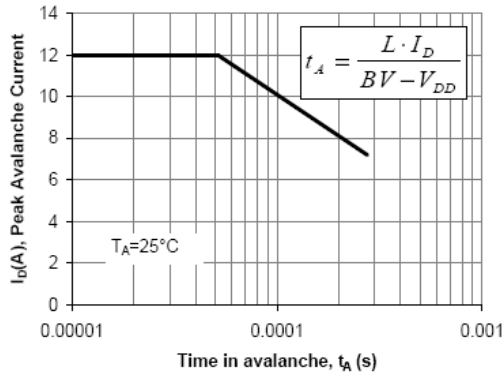


Figure 12: Single Pulse Avalanche capability

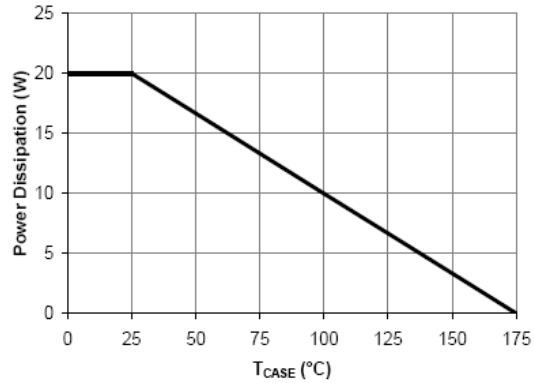


Figure 13: Power De-rating (Note B)

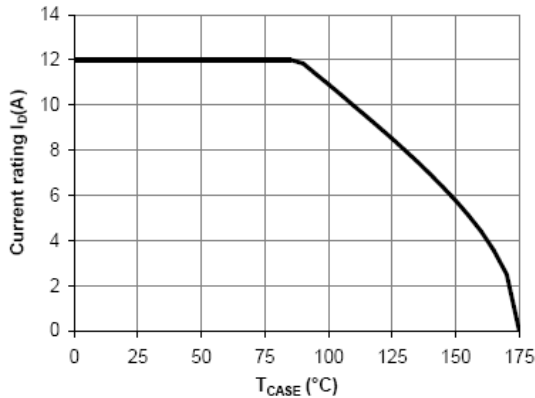


Figure 14: Current De-rating (Note B)

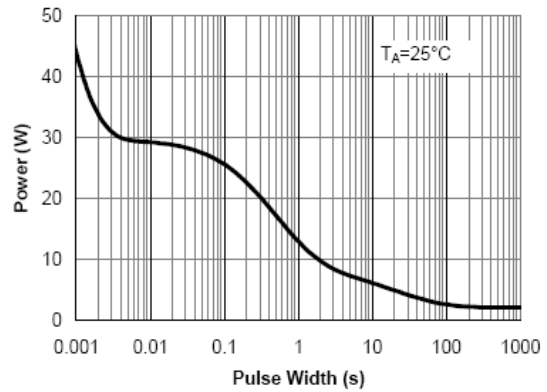


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

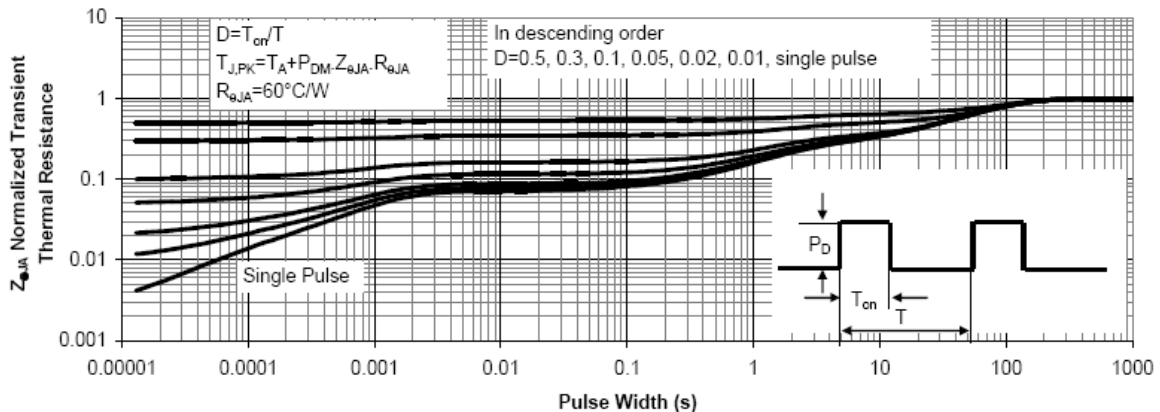
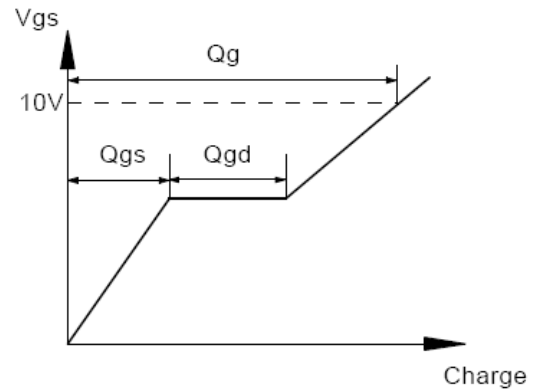
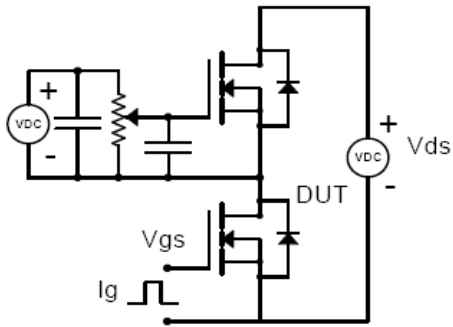
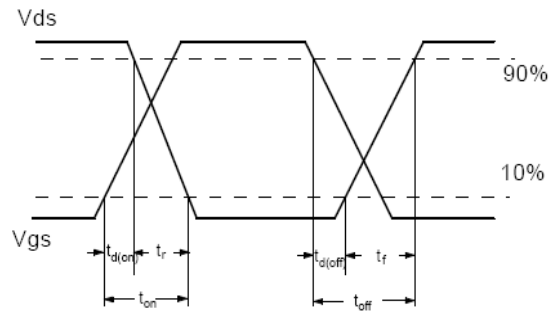
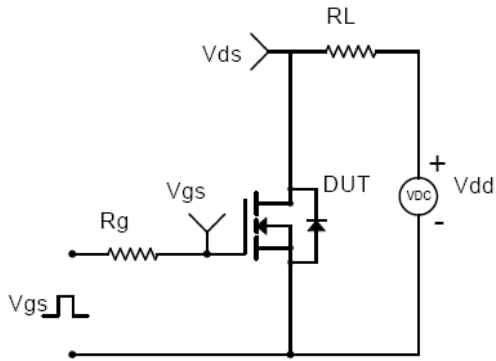


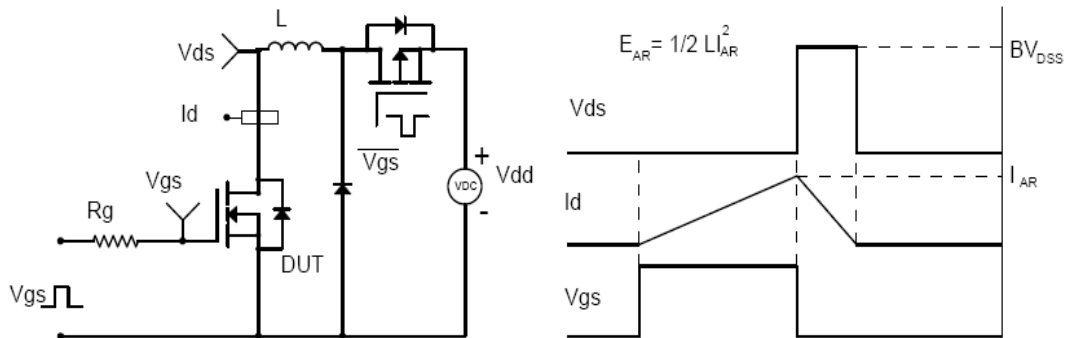
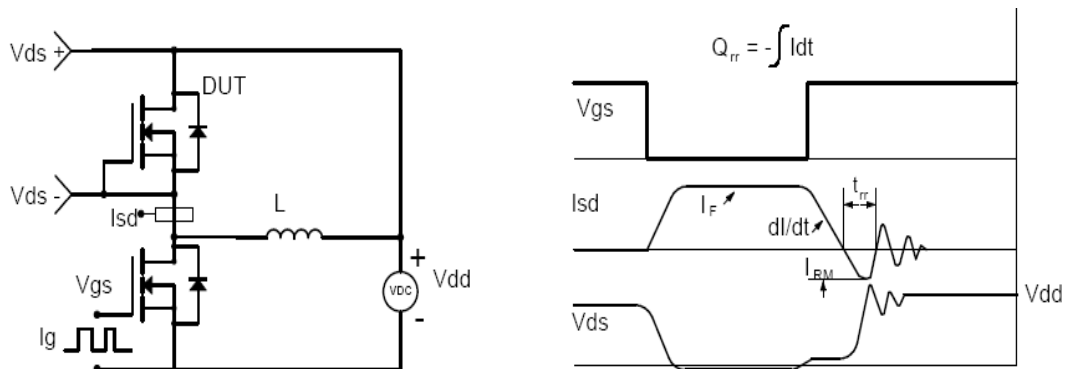
Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

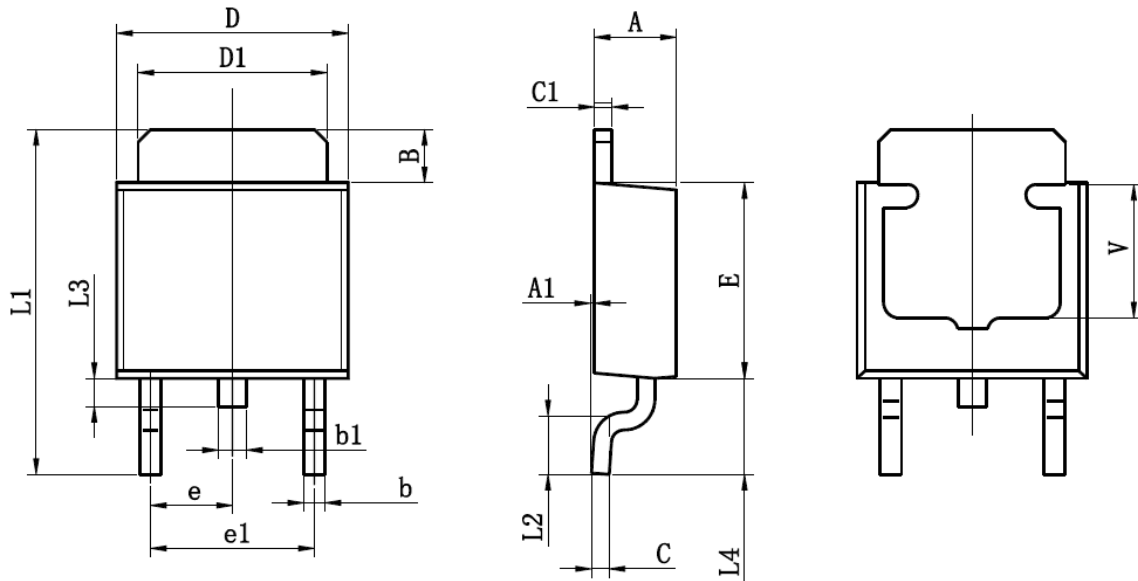
GATE CHARGE TEST CIRCUIT & WAVEFORM



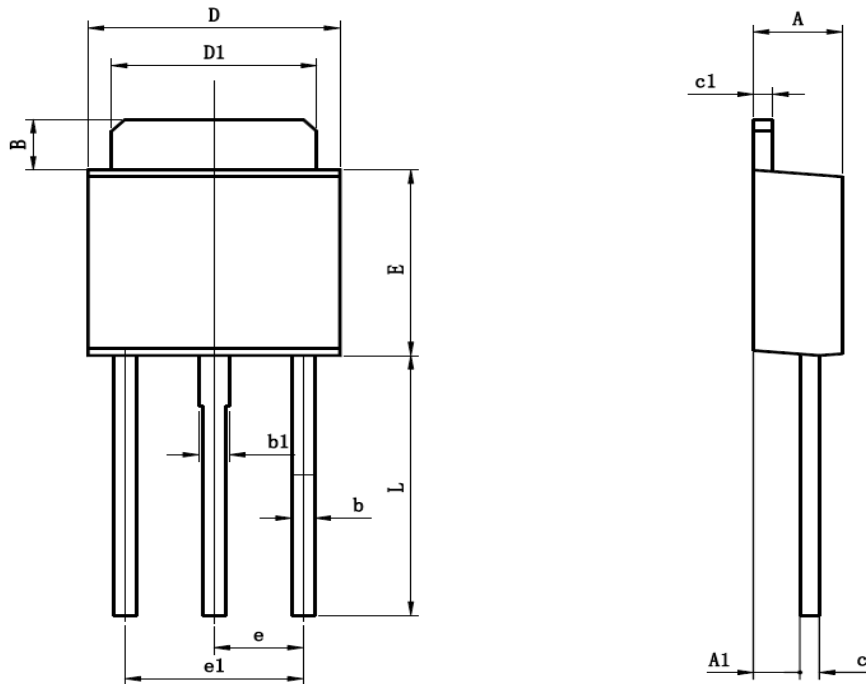
RESISTIVE SWITCHING TEST CIRCUIT & WAVEFORMS



UNCLAMPED INDUCTIVE SWITCHING (UIS) TEST CIRCUIT & WAVEFORMS

DIODE RECOVERY TEST CIRCUIT & WAVEFORMS


TO-252-2L PACKAGE OUTLINE SOP-8P


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L1	9.500	9.900	0.374	0.390
L2	1.400	1.780	0.055	0.070
L3	0.650	0.950	0.026	0.037
L4	2.550	2.900	0.100	0.114
V	3.80REF		0.150REF	

TO-251 PACKAGE OUTLINE SOP-8P


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	2.200	2.400	0.087	0.094
A1	1.020	1.270	0.040	0.050
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300TYP		0.091TYP	
e1	4.500	4.700	0.177	0.185
L	7.500	7.900	0.295	0.311