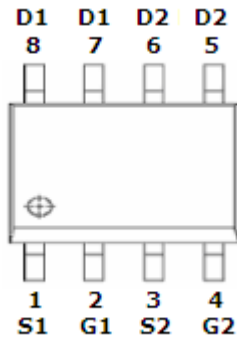


DESCRIPTION

The STC4606 is the N & P-Channel enhancement mode power field effect transistor using high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. This device is particularly suited for low voltage application such as notebook computer power management and other battery powered circuits, where high-side switching, low in-line power loss and resistance to transient are needed.

PIN CONFIGURATION SOP-8



PART MARKING SOP-8



Y : Year A : Date Code

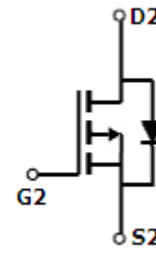
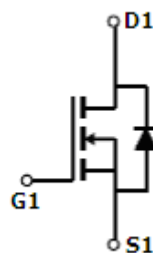
FEATURE

N-Channel

- 30V/6.9A, $R_{DS(ON)} = 30m\Omega$ (Typ)
@ $V_{GS} = 10V$
- 30V/6.0A, $R_{DS(ON)} = 46m\Omega$
@ $V_{GS} = 4.5V$

P-Channel

- -30V/-6.0A, $R_{DS(ON)} = 41m\Omega$ (Typ)
@ $V_{GS} = -10V$
- -30V/-5.0A, $R_{DS(ON)} = 60m\Omega$
@ $V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package





STC4606 

N&P Pair Enhancement Mode MOSFET

6.5A / -6.9A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical		Unit
		N	P	
Drain-Source Voltage	V _{DSS}	30	-30	V
Gate-Source Voltage	V _{GSS}	±20	±20	V
Continuous Drain Current (T _J =150°C)	I _D	T _A =25°C 6.5	-6.9	A
		T _A =70°C 5.8	-5.0	
Pulsed Drain Current	I _{DM}	26	-30	A
Continuous Source Current (Diode Conduction)	I _S	3.0	-3.0	A
Power Dissipation	P _D	T _A =25°C 2.0	2.0	W
		T _A =70°C 1.44	1.44	
Operation Junction Temperature	T _J	150		°C
Storage Temperature Range	T _{STG}	-55/150		°C
Thermal Resistance-Junction to Ambient	R _{θJA}	T ≤ 10Sec 62.5	62.5	°C/W
		Steady State 110	110	



STC4606  Lead-free

N&P Pair Enhancement Mode MOSFET

6.5A / -6.9A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$ $V_{GS}=0V, I_D=-250\mu A$	N P	30 -30		V	
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$ $V_{DS}=V_{GS}, I_D=-250\mu A$	N P	1.0 -1.0	3.0 -3.0	V	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$ $V_{DS}=0V, V_{GS}=\pm 20V$	N P		± 100 ± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS} $T_J=55^\circ C$	$V_{DS}=24V, V_{GS}=0V$ $V_{DS}=-24V, V_{GS}=0V$ $V_{DS}=24V, V_{GS}=0V$ $V_{DS}=-24V, V_{GS}=0V$	N P N P		1 -1 5 -5	μA	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$ $V_{DS} \leq -5V, V_{GS}=-10V$	N P	26 -30		A	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=6.9A$ $V_{GS}=-10V, I_D=-6.0A$ $V_{GS}=4.5V, I_D=5.0A$ $V_{GS}=-4.5V, I_D=-5.0A$	N P N P		0.030 0.041 0.046 0.060	0.040 0.056 0.055 0.072	Ω
Forward Tran Conductance	g_{fs}	$V_{DS}=5V, I_D=6.9A$ $V_{DS}=-15V, I_D=-5.9A$	N P		15 13	S	
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$ $I_S=-1.7A, V_{GS}=0V$	N P		0.76 -0.76	1.0 -1.0	V
Dynamic							
Total Gate Charge	Q_g	N-Channel $V_{DS}=15V, V_{GS}=10V$ $I_D=6.9A$ P-Channel $V_{DS}=-15V, V_{GS}=-10V$ $I_D=5.0A$	N P		13.8 18.5	16.6 22.2	nC
Gate-Source Charge	Q_{gs}		N P		1.8 2.7		
Gate-Drain Charge	Q_{gd}		N P		2.0 4.5		
Turn-On Time	$t_{d(on)}$ t_r	N-Channel $V_{DS}=10V, R_L=2.2\Omega$ $I_D=1A, V_{GEN}=10V$ $R_G=3\Omega$ P-Channel $V_{DS}=-10V, R_L=2.7\Omega$ $I_D=-1A, V_{GEN}=-3V$ $R_G=2.7\Omega$	N P N P		4.6 7.7 4.1 5.7	7 11.5 6 8.5	nS
Turn-Off Time	$t_{d(off)}$ t_f		N P		20.6 20.2	30 30	
			N P		5.2 9.5	8 14	

TYPICAL CHARACTERISTICS (N MOS)

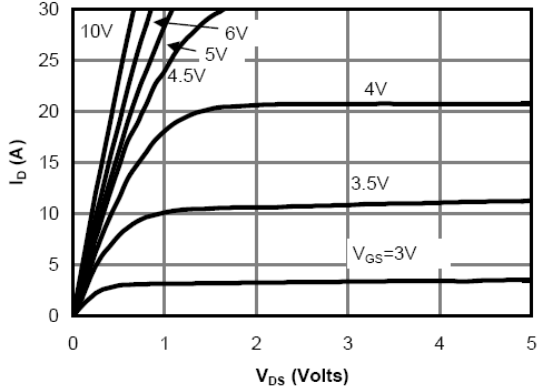


Figure 1: On-Region Characteristics

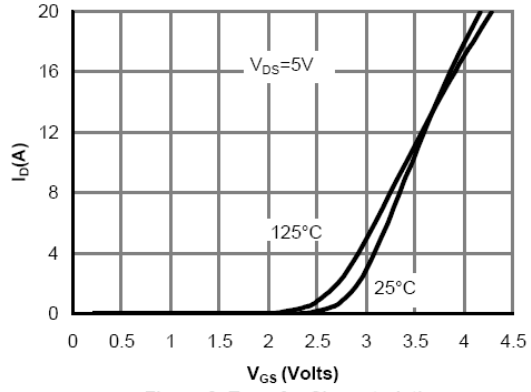


Figure 2: Transfer Characteristics

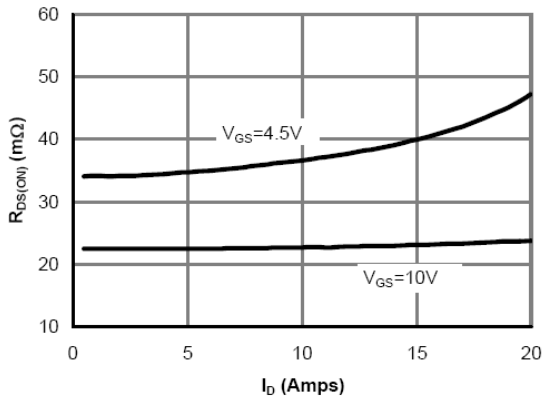


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

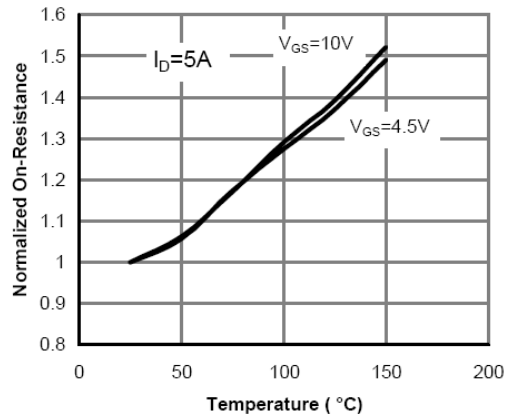


Figure 4: On-Resistance vs. Junction Temperature

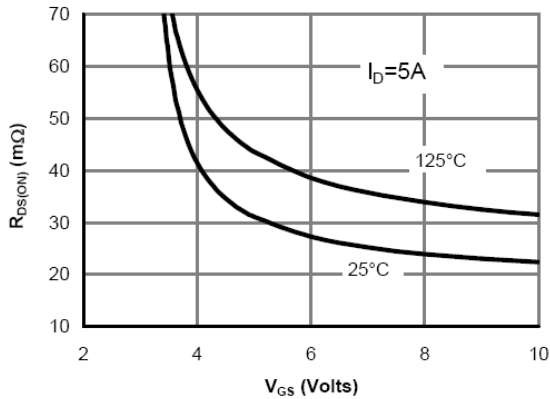


Figure 5: On-Resistance vs. Gate-Source Voltage

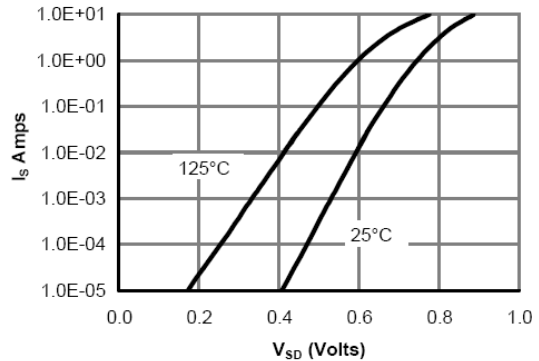


Figure 6: Body diode characteristics

TYPICAL CHARACTERISTICS (N MOS)

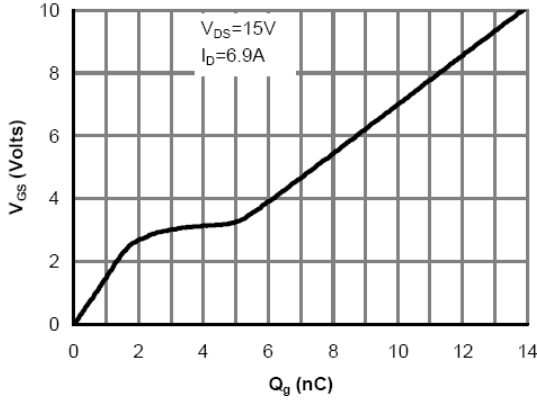


Figure 7: Gate-Charge characteristics

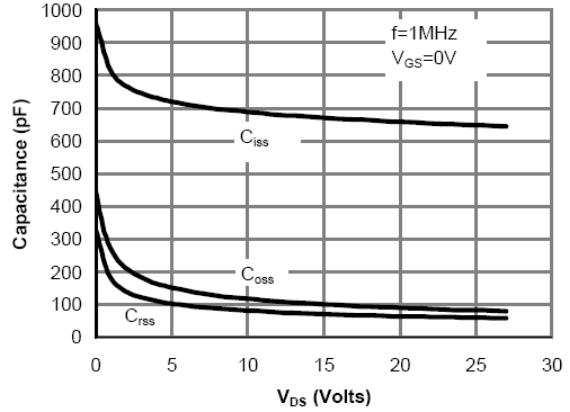


Figure 8: Capacitance Characteristics

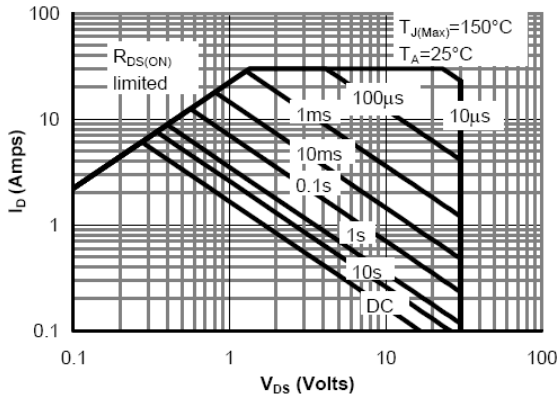


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

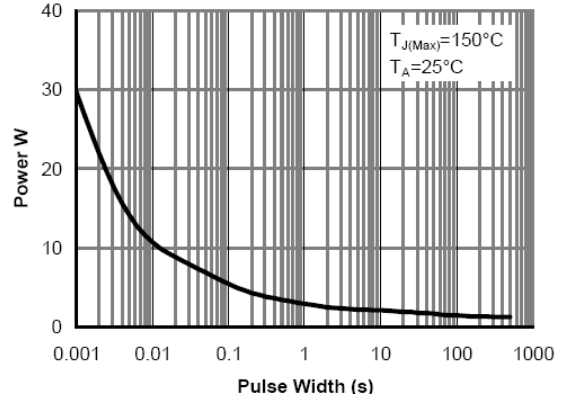


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

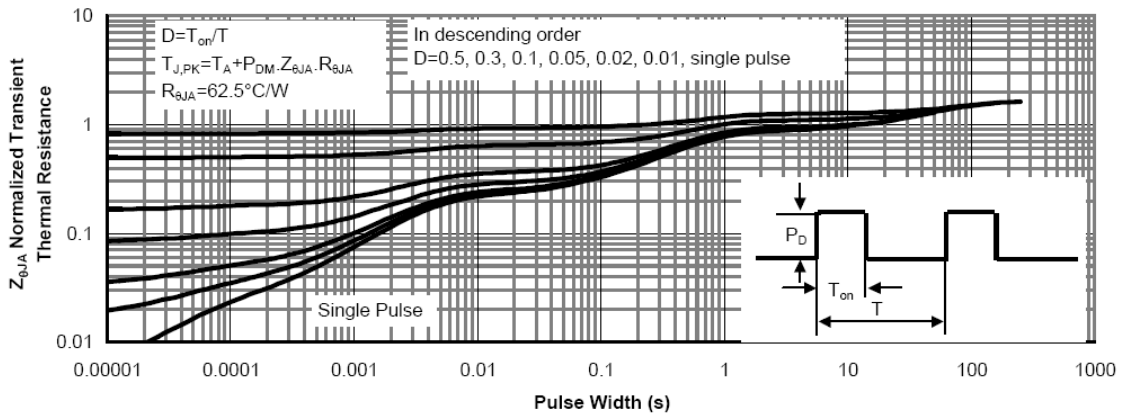


Figure 11: Normalized Maximum Transient Thermal Impedance

TYPICAL CHARACTERISTICS (P MOS)

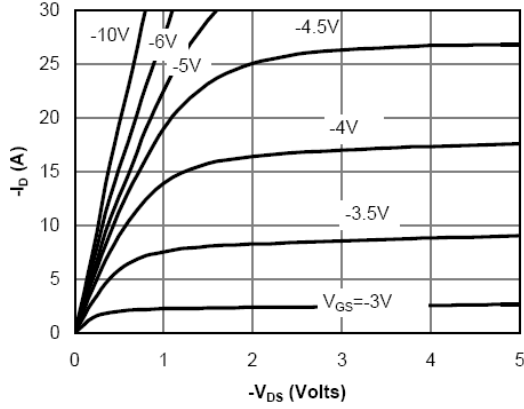


Fig 1: On-Region Characteristics

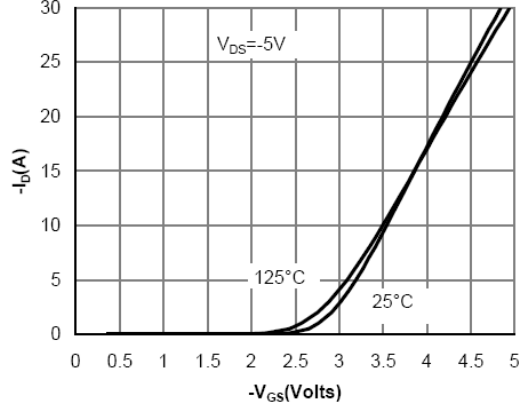


Figure 2: Transfer Characteristics

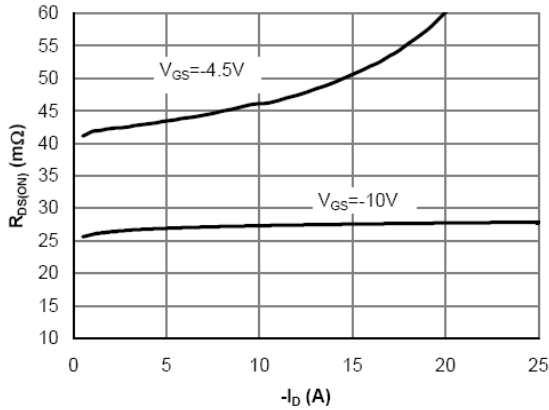


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

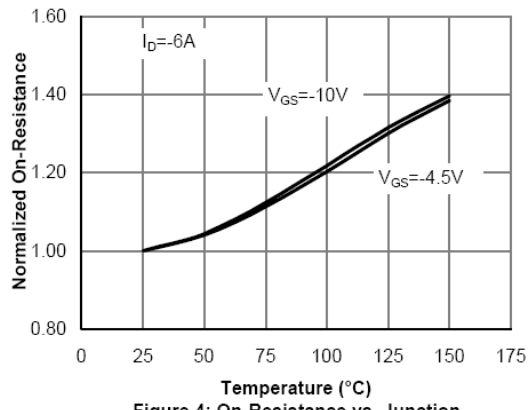


Figure 4: On-Resistance vs. Junction Temperature

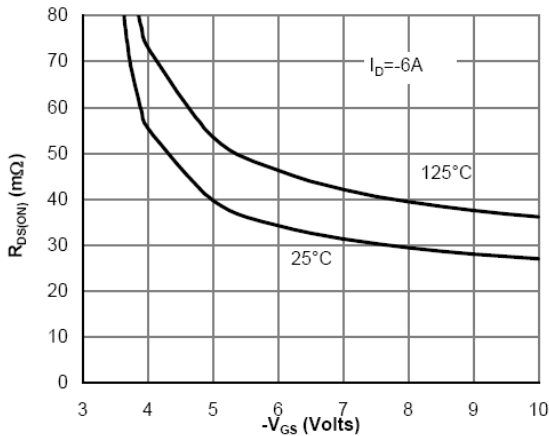


Figure 5: On-Resistance vs. Gate-Source Voltage

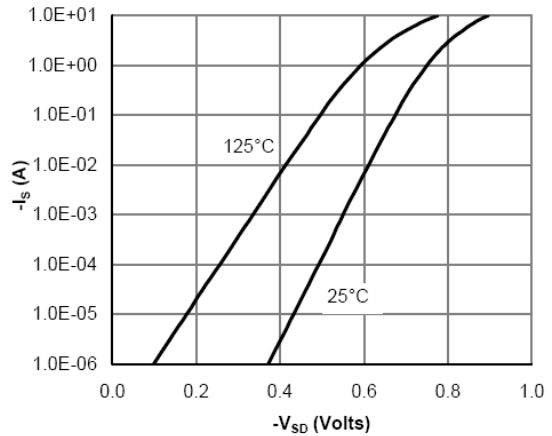


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS (P MOS)

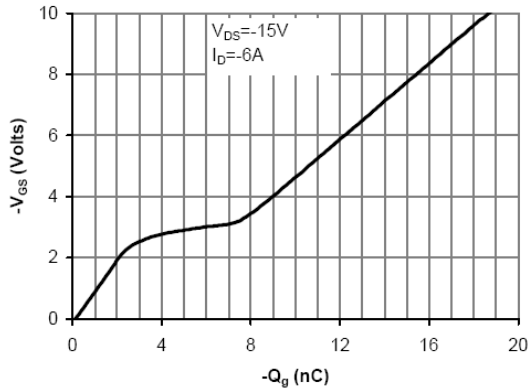


Figure 7: Gate-Charge Characteristics

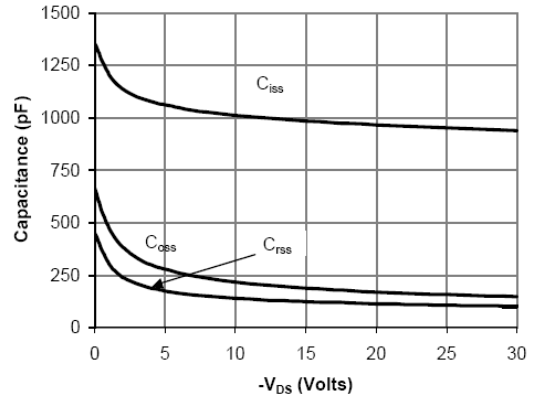


Figure 8: Capacitance Characteristics

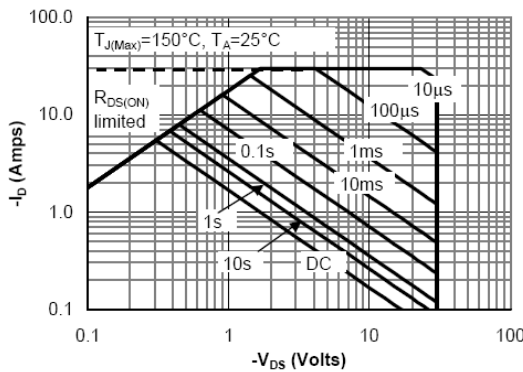


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

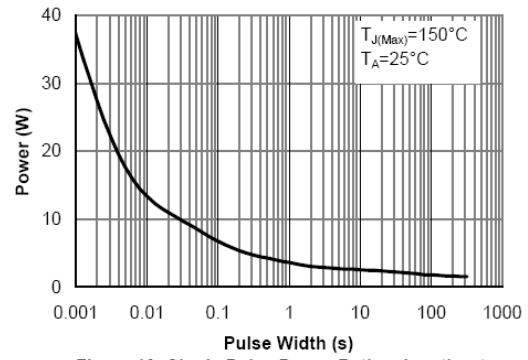


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

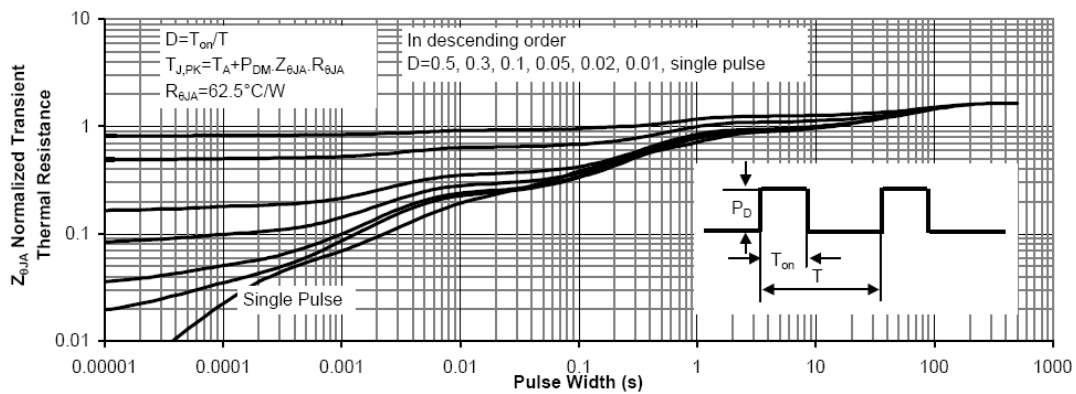
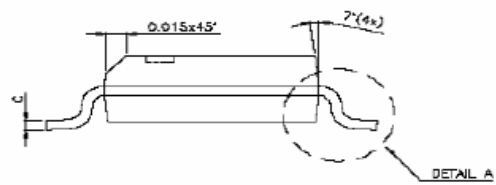
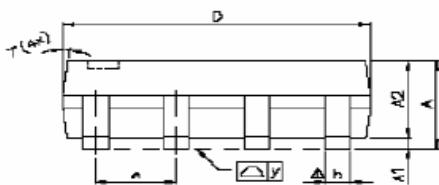
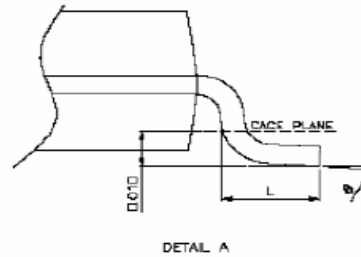
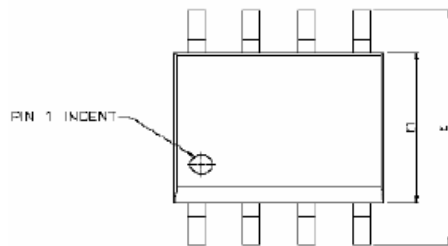


Figure 11: Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE OUTLINE


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
ϕ	0°	—	8°	0°	—	8°