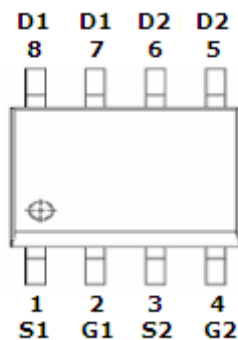
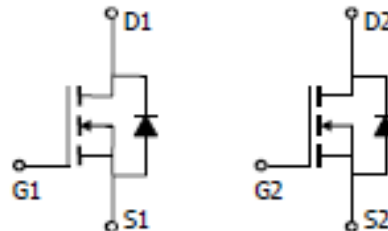


DESCRIPTION

STN4822 is the Dual N-Channel logic enhancement mode power field effect transistors which are produced using high cell density DMOS trench technology. It is suitable for the power management applications in the portable or battery powered system.

**PIN CONFIGURATION
SOP-8**

FEATURE

- 30V/8.5A, $R_{DS(ON)} = 16m\Omega$ (Typ.) @VGS = 10V
- 30V/6.6A, $R_{DS(ON)} = 26m\Omega$ @VGS = 4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

**PART MARKING
SOP-8**


Y:Year Code A: Process Code



STN4822 

Dual N Channel Enhancement Mode MOSFET
8.5A

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	30	V
Gate-Source Voltage	V _{GSS}	±20	V
Continuous Drain Current (T _J =150°C)	I _D	T _A =25°C 8.5	A
		T _A =70°C 6.6	
Pulsed Drain Current	I _{DM}	30	A
Continuous Source Current (Diode Conduction)	I _S	3.0	A
Power Dissipation	P _D	T _A =25°C 2.0	W
		T _A =70°C 1.28	
Operation Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	48	°C/W



STN4822 

Dual N Channel Enhancement Mode MOSFET
8.5A

ELECTRICAL CHARACTERISTICS (Ta = 25°C Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.8	3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			100	nA
Zero Gate Voltage Drain Current	I_{DSS} $T_J=55^\circ C$	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 10V, V_{GS}=5V$	30			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=8.5A$ $V_{GS}=4.5V, I_D=6.6A$		13 20	17 26	$m\Omega$
Forward Tran Conductance	g_{fs}	$V_{DS}=5.0V, I_D=8.5A$		23		S
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$		0.76	1.0	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, V_{GS}=10V$ $I_D=8.5A$		15	23	nC
Gate-Source Charge	Q_{gs}			2.6		
Gate-Drain Charge	Q_{gd}			2.78		
Input Capacitance	C_{iss}	$V_{DS}=15.0V, V_{GS}=0V$ $f=1MHz$		805	1200	pF
Output Capacitance	C_{oss}			145		
Reverse Transfer Capacitance	C_{rss}			112		
Turn-On Time	$t_{d(on)}$ t_r	$V_{DS}=15V, R_L=1.8\Omega$ $I_D=1A, V_{GEN}=10V$ $R_G=3\Omega$		5.2	6.5	nS
Turn-Off Time	$t_{d(off)}$ t_f			6	7.5	
				19.3	25	
				4.3	6	

TYPICAL CHARACTERISTICS (25°C Unless Note)

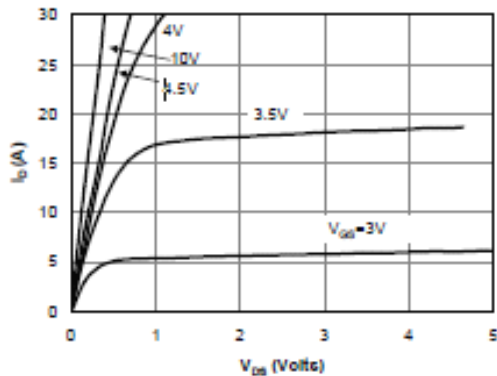


Fig 1: On-Region Characteristics

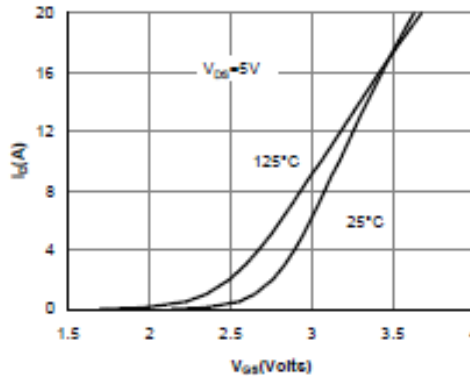


Figure 2: Transfer Characteristics

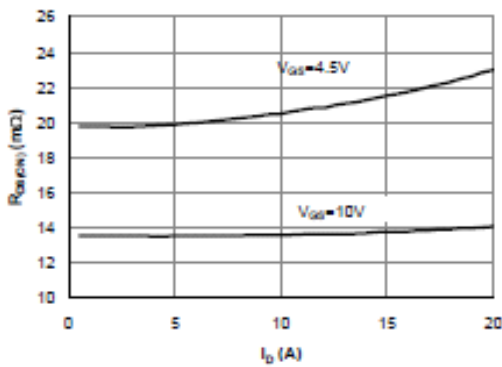


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

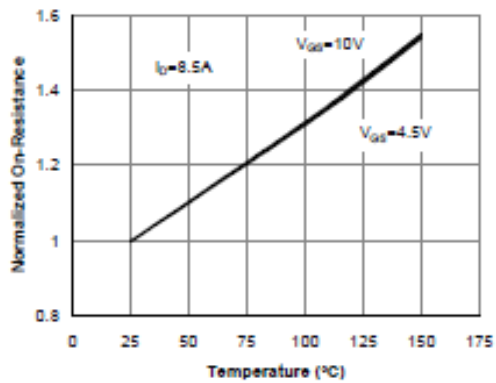


Figure 4: On-Resistance vs. Junction Temperature

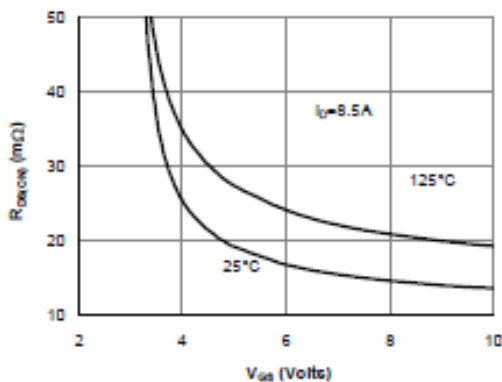


Figure 5: On-Resistance vs. Gate-Source Voltage

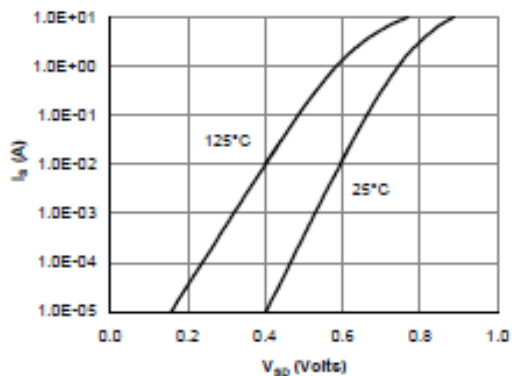


Figure 6: Body-Diode Characteristics

TYPICAL CHARACTERISTICS (25°C Unless Note)

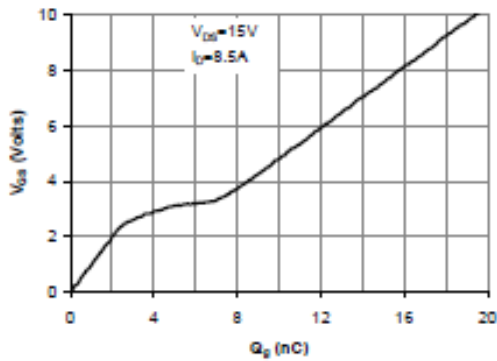


Figure 7: Gate-Charge Characteristics

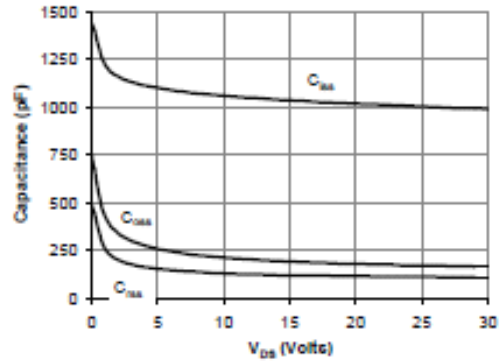


Figure 8: Capacitance Characteristics

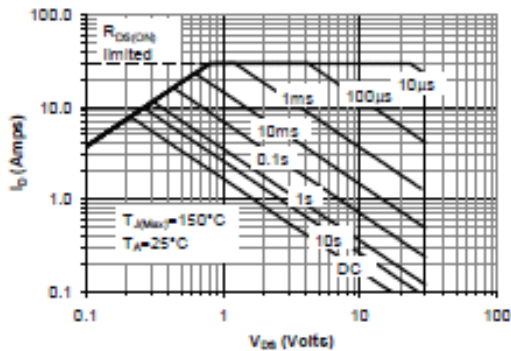


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

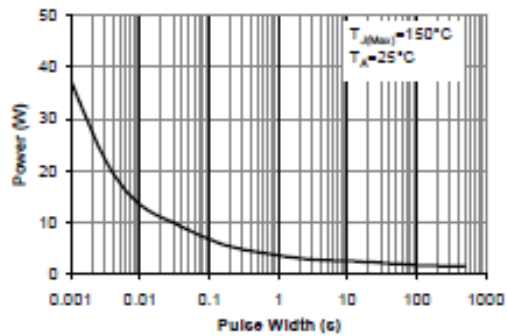


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

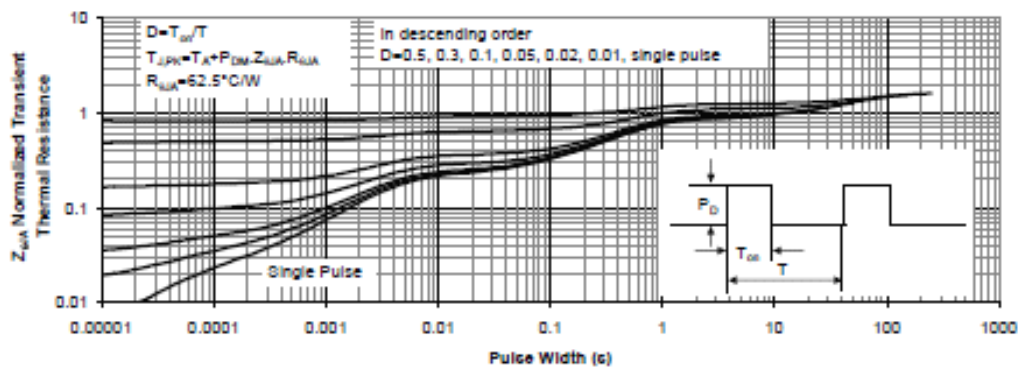
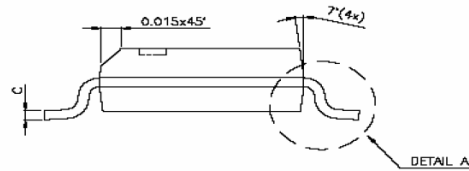
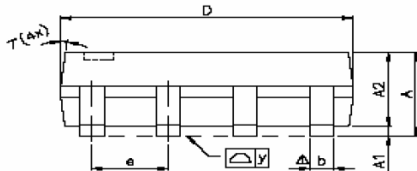
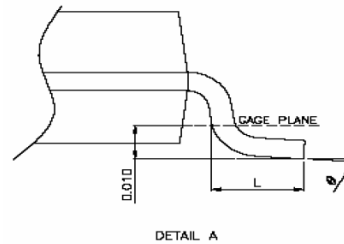
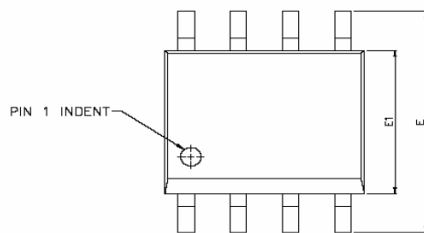


Figure 11: Normalized Maximum Transient Thermal Impedance

SOP-8 PACKAGE OUTLINE


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
Δ y	—	—	0.076	—	—	0.003
\varnothing	0°	—	8°	0°	—	8°