STP9235

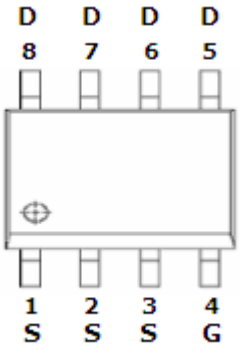
P Channel Enhancement Mode MOSFET

- 7.5A

DESCRIPTION

STP9235 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.

PIN CONFIGURATION
SOP-8

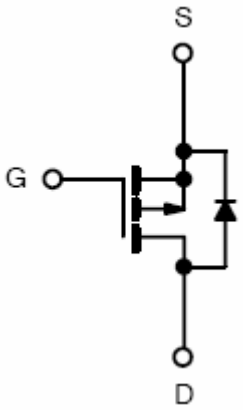


FEATURE

- -25V/-7.5A, $R_{DS(ON)}$ = 45mΩ @V_{GS} = -10V
- -25V/-6.0A, $R_{DS(ON)}$ = 55mΩ @V_{GS} = -6.0V
- -25V/-5.4A, $R_{DS(ON)}$ = 65mΩ @V_{GS} = -4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PART MARKING
SOP-8

S : Subcontractor Y : Year Code
A : Process Code



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ABSOULTE MAXIMUM RATINGS (Ta = 25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		VDSS	-25	V
Gate-Source Voltage		VGSS	±20	V
Continuous Drain Current (TJ=150℃)	TA=25℃ TA=70℃	ID	-8.0 -6.0	A
Pulsed Drain Current		IDM	-30	A
Continuous Source Current (Diode Conduction)		IS	-2.3	A
Power Dissipation	TA=25℃ TA=70℃	PD	2.8 1.6	W
Operation Junction Temperature		TJ	-55/150	℃
Storgae Temperature Range		TSTG	-55/150	℃
Thermal Resistance-Junction to Ambient		RθJA	70	℃/W

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ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=-250uA	-25			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=-250uA	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-18V,V_{GS}=0V			-1	uA
		V_{DS}=-18V,V_{GS}=0V T_J=85℃			-5	
On-State Drain Current	$I_{D(on)}$	V_{DS}=-5V,V_{GS}=-4.5V	-10			A
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-7.5A V_{GS}=-6.0V,I_D=-6.0A V_{GS}=-4.5V,I_D=-5.4A		35 45 55	45 55 65	mΩ
Forward Transconductance	gfs	V_{DS}=-15V,I_D=-5.7V		13		S
Diode Forward Voltage	V_{SD}	I_S=-2.3A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-15V,V_{GS}=-10V I_D≡-3.5A		16	24	nC
Gate-Source Charge	Q_{gs}			2.3		
Gate-Drain Charge	Q_{gd}			4.5		
Input Capacitance	C_{iss}	V_{DS} ==-15V,VGS=0V f=1MHz		680		pF
Output Capacitance	C_{oss}			120		
Reverse TransferCapacitance	C_{rss}			75		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V,R_L=15Ω I_D=-1A,V_{GEN}=-10V R_G=6Ω		14	25	nS
	tr			15	26	
Turn-Off Time	$t_{d(off)}$			42	70	
	tf			30	50	

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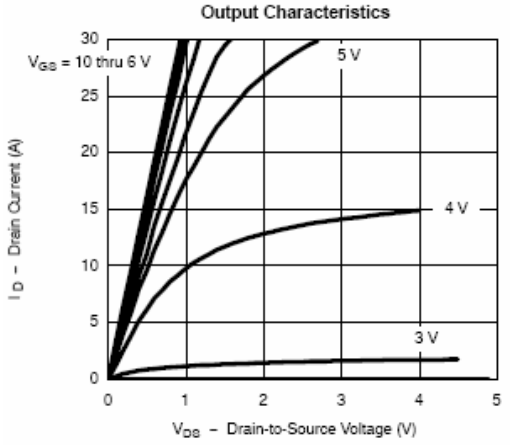
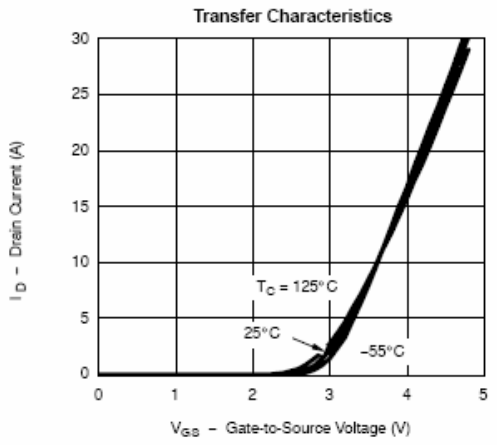
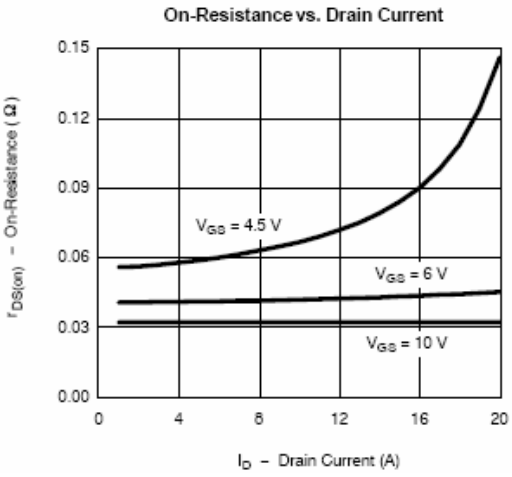
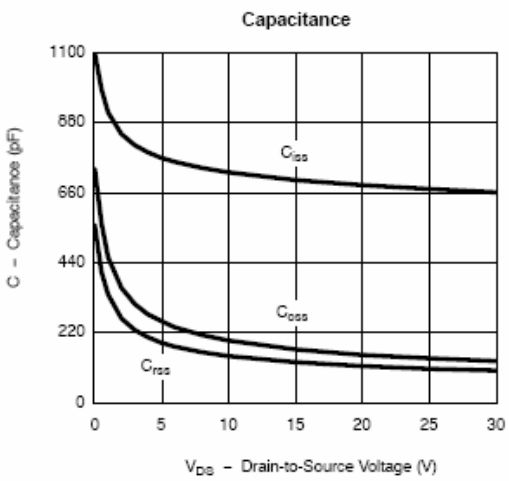
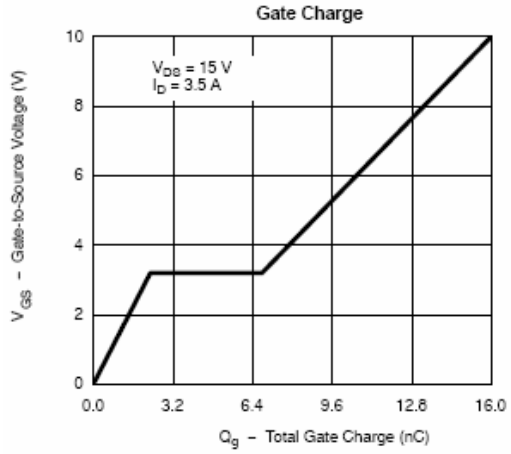
TYPICAL CHARACTERICTICS

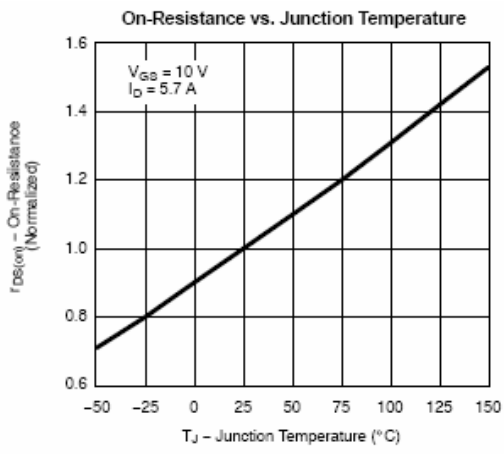












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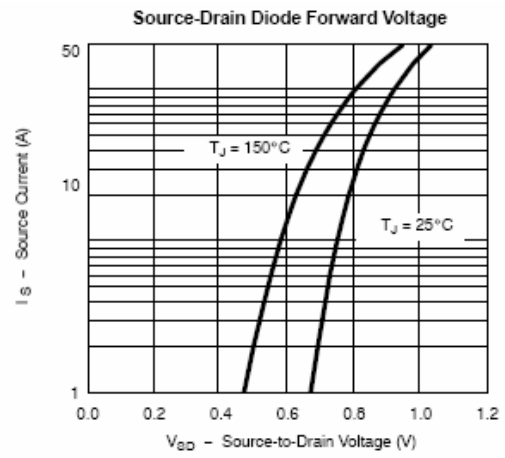

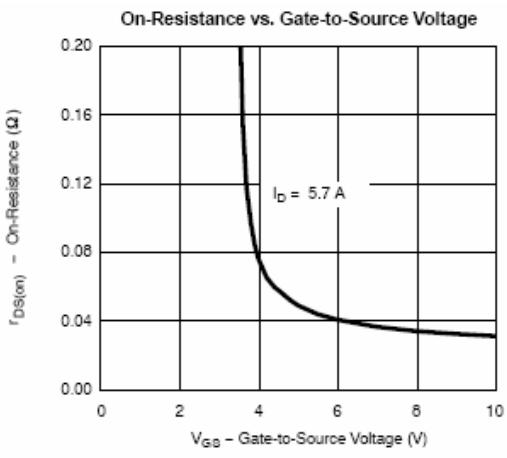

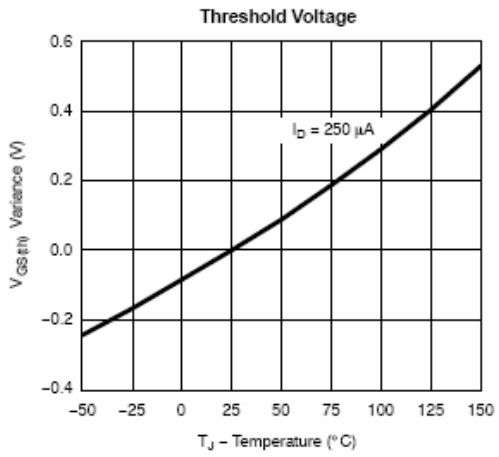

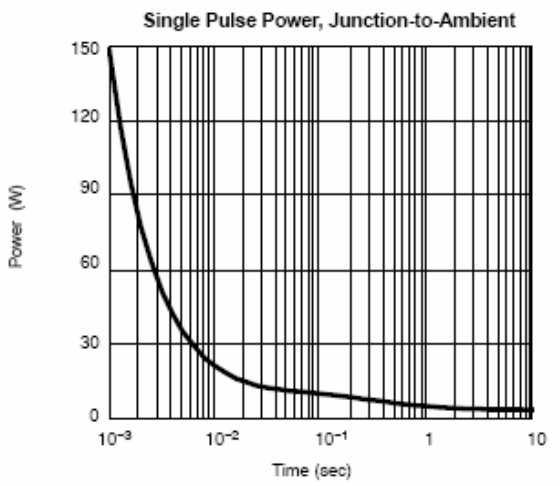

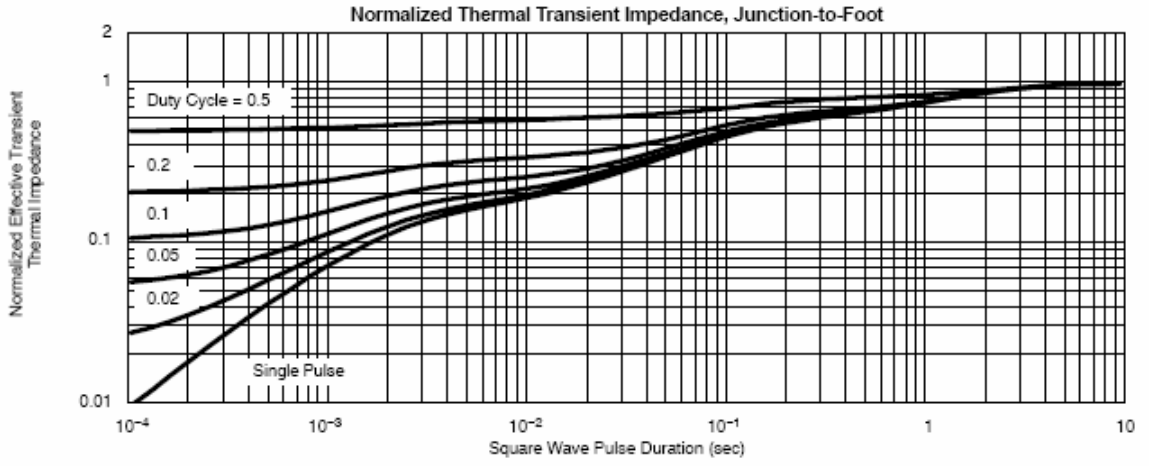

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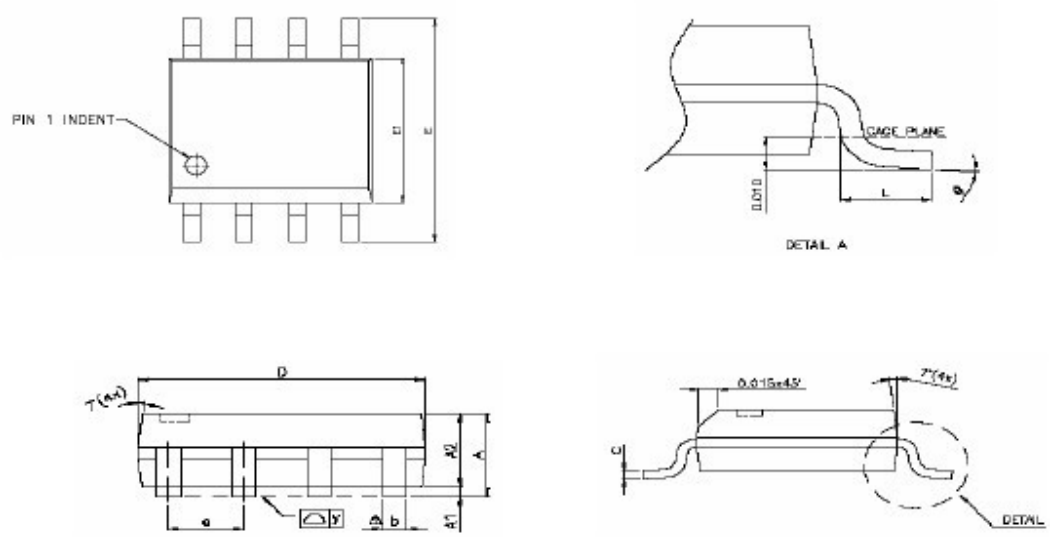
PACKAGE OUTLINE SOP-8P



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
② y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°

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