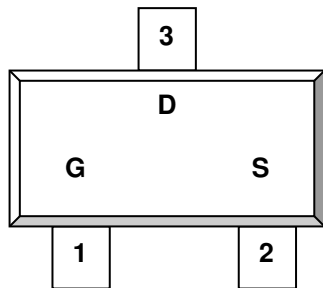
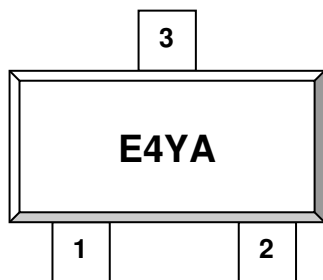


**DESCRIPTION**

The ST10E4 is the N-Channel logic enhancement mode power field effect transistor is produce using high cell density, DMOS trench technology. This high-density process is especially tailored to minimize on-state resistance. These device are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high side switching.

**PIN CONFIGURATION**  
**SOT-23-3L**


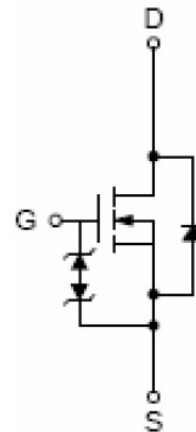
1.Gate 2.Source 3.Drain

**PART MARKING**  
**SOT-23-3L**


Y: Year Code A: Praduce Code

**FEATURE**

- 100V/3.0A,  $R_{DS(ON)} = 160m\Omega$   
@ $V_{GS} = 10V$
- 100V/2.5A,  $R_{DS(ON)} = 180m\Omega$   
@ $V_{GS} = 4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-3L package design



**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

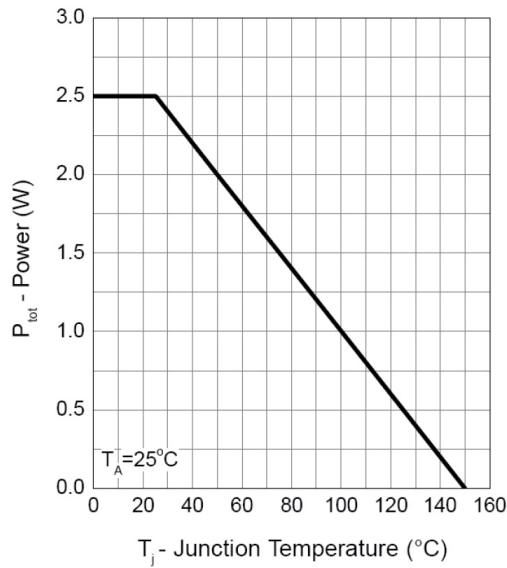
Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	100	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current T <sub>J</sub> =150°C	I <sub>D</sub>	T <sub>A</sub> =25°C 3.0	A
		T <sub>A</sub> =70°C 2.1	
Pulsed Drain Current	I <sub>DM</sub>	10	A
Continuous Source Current (Diode Conduction)	I <sub>S</sub>	1.7	A
Power Dissipation	P <sub>D</sub>	T <sub>A</sub> =25°C 1.5	W
		T <sub>A</sub> =70°C 1.0	
Avalanche Energy, Single Plused	L=0.3mH E <sub>AS</sub>	25	mJ
Operation Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	75	°C/W

**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

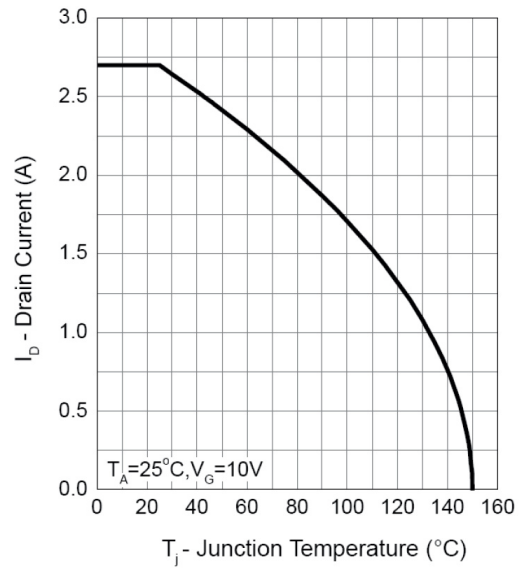
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 30$	$\mu A$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$			1	$\mu A$
		$V_{DS}=80V, V_{GS}=0V$ $T_J=55^\circ C$			10	
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=3.0A$ $V_{GS}=4.5V, I_D=2.0A$		153 168	160 180	$m\Omega$
Diode Forward Voltage	$V_{SD}$	$I_S=1.7A, V_{GS}=0V$			1.0	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=50V$ $V_{GS}=10V$ $I_D=2.0A$		10	15	nC
Gate-Source Charge	$Q_{gs}$			1.9		
Gate-Drain Charge	$Q_{gd}$			2.8		
Input Capacitance	$C_{iss}$	$V_{DS}=30V$ $V_{GS}=0V$ $F=1MHz$		455		pF
Output Capacitance	$C_{oss}$			43		
Reverse Transfer Capacitance	$C_{rss}$			28		
Turn-On Time	$t_{d(on)tr}$	$V_{DD}=30V$ $R_L=30\Omega$ $I_D=1.0A$ $V_{GEN}=10V$ $R_G=6\Omega$		11	21	nS
				10	19	
Turn-Off Time	$t_{d(off)tf}$			24	44	
				21	39	

**TYPICAL CHARACTERISTICS** (25°C Unless noted)

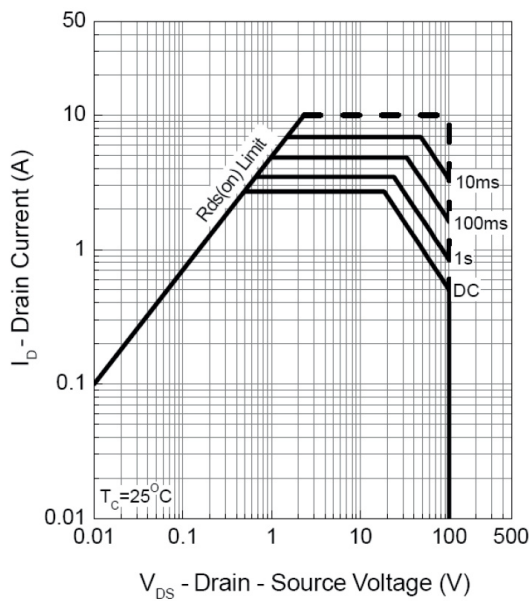
**Power Dissipation**



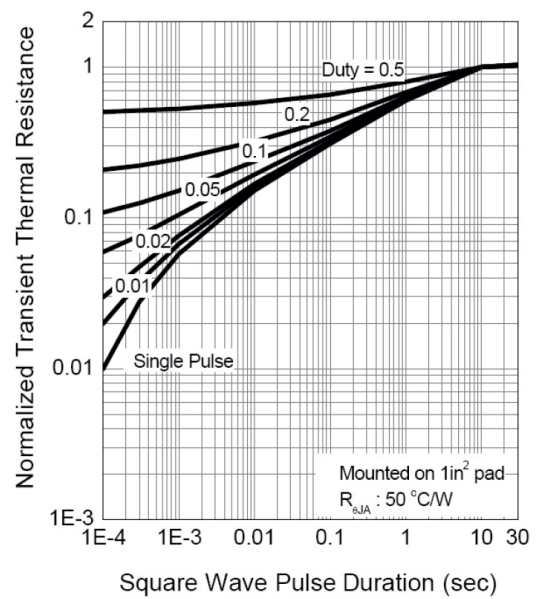
**Drain Current**



**Safe Operation Area**

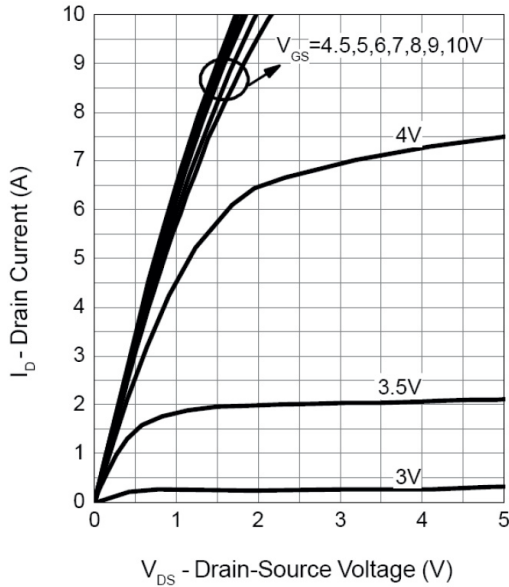


**Thermal Transient Impedance**

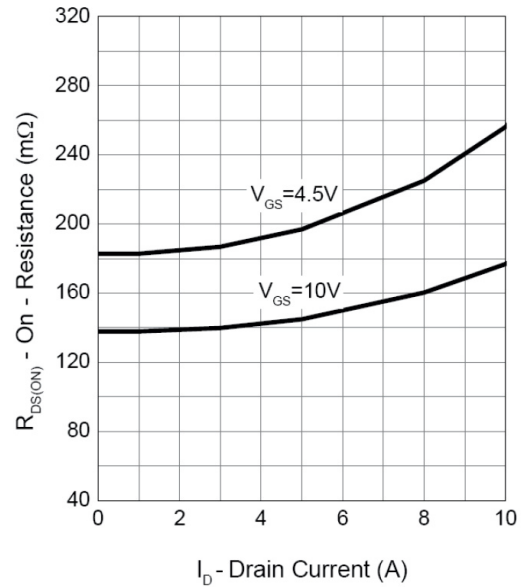


**TYPICAL CHARACTERISTICS** (25°C Unless noted)

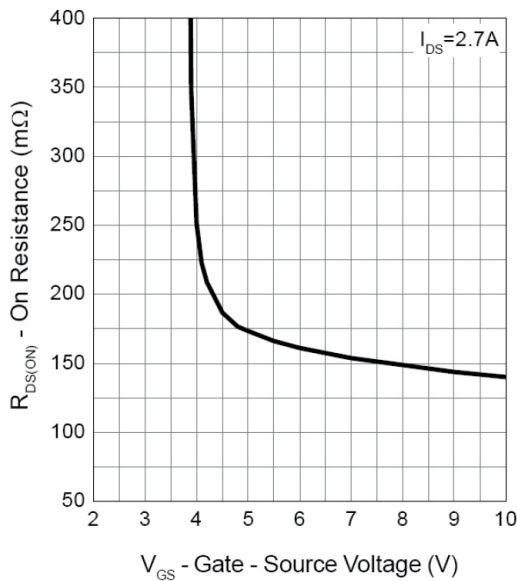
**Output Characteristics**



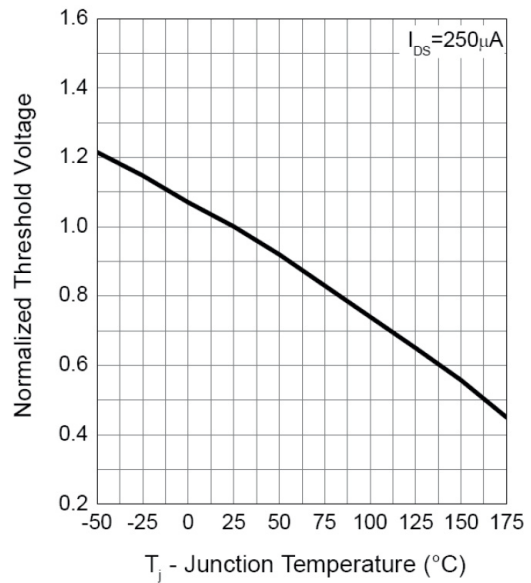
**Drain-Source On Resistance**



**Gate-Source On Resistance**

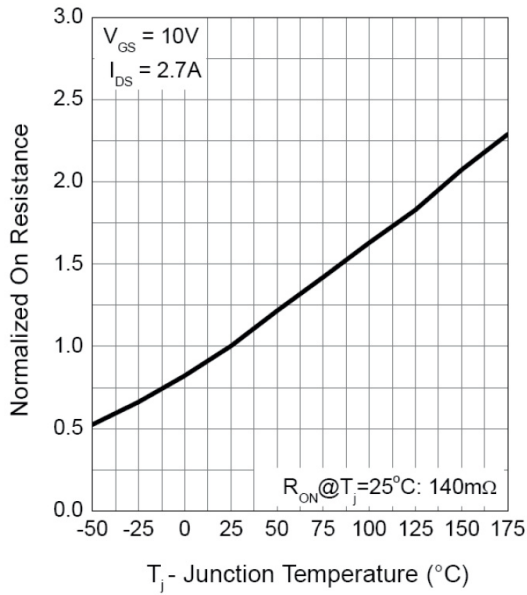


**Gate Threshold Voltage**

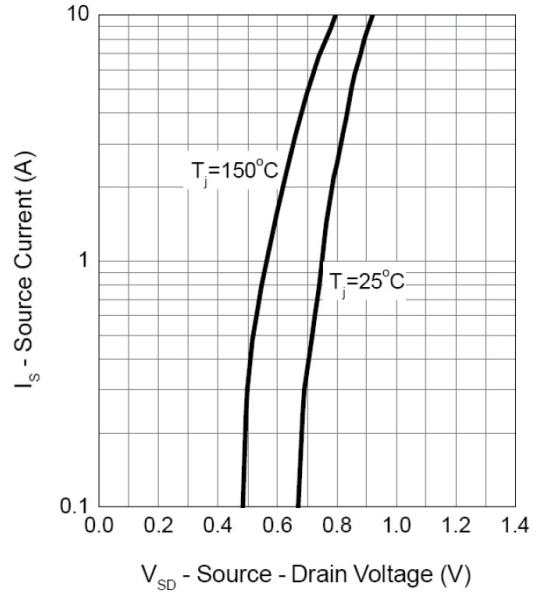


**TYPICAL CHARACTERISTICS (25°C Unless noted)**

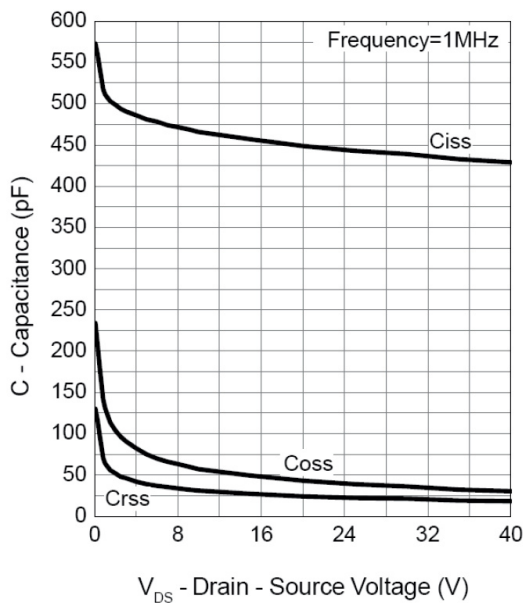
**Drain-Source On Resistance**



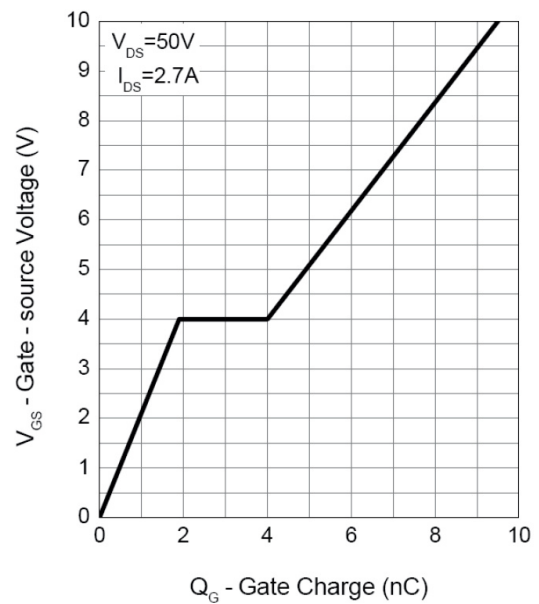
**Source-Drain Diode Forward**

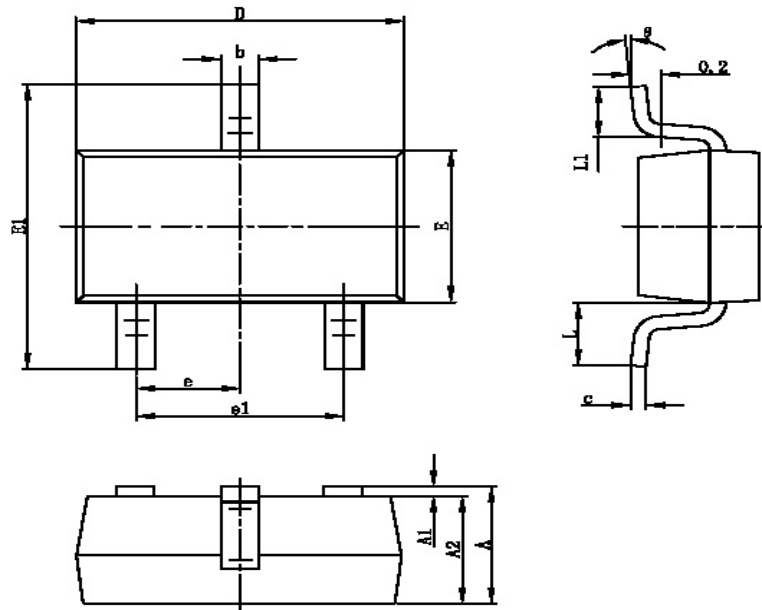


**Capacitance**



**Gate Charge**



**SOT-23-3L PACKAGE OUTLINE**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°