

MOSFETs Silicon P-Channel MOS (U-MOSVI)

# **TJ10S04M3L**

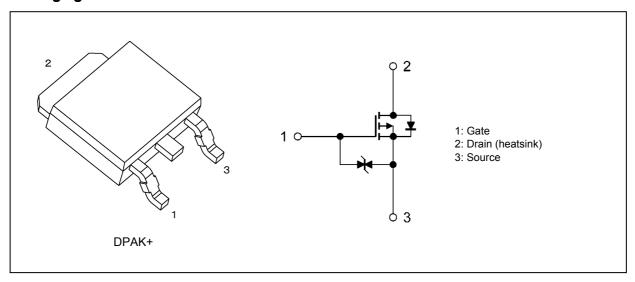
#### 1. Applications

- Automotive
- · Motor Drivers
- · DC-DC Converters
- · Switching Voltage Regulators

#### 2. Features

- (1) Low drain-source on-resistance:  $R_{DS(ON)} = 33.8 \text{ m}\Omega$  (typ.) ( $V_{GS} = -10 \text{ V}$ )
- (2) Low leakage current:  $I_{DSS} = -10 \mu A \text{ (max) (V}_{DS} = -40 \text{ V)}$
- (3) Enhancement mode:  $V_{th}$  = -2.0 to -3.0 V ( $V_{DS}$  = -10 V,  $I_D$  = -1 mA)

#### 3. Packaging and Internal Circuit



# 4. Absolute Maximum Ratings (Note) (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics				Rating	Unit
Drain-source voltage			$V_{DSS}$	-40	V
Gate-source voltage			V <sub>GSS</sub>	-20/+10	
Drain current (DC)		(Note 1)	I <sub>D</sub>	-10	Α
Drain current (pulsed)		(Note 1)	I <sub>DP</sub>	-20	
Power dissipation	(T <sub>c</sub> = 25°C)		P <sub>D</sub>	27	W
Single-pulse avalanche energy		(Note 2)	E <sub>AS</sub>	23	mJ
Avalanche current			I <sub>AR</sub>	-10	Α
Channel temperature		(Note 3)	T <sub>ch</sub>	175	°C
Storage temperature		(Note 3)	T <sub>stg</sub>	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



#### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	R <sub>th(ch-c)</sub>	5.4	°C/W

Note 1: Ensure that the channel temperature does not exceed 175°C.

Note 2:  $V_{DD}$  = -25 V,  $T_{ch}$  = 25°C (initial), L = 243  $\mu H$ ,  $R_{G}$  = 25  $\Omega$ ,  $I_{AR}$  = -10 A

Note 3: The definitions of the absolute maximum channel and storage temperatures are qualified per AEC-Q101.

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.



#### 6. Electrical Characteristics

## 6.1. Static Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> = -16/+10 V, V <sub>DS</sub> = 0 V	_	_	±10	μА
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = -40 V, V <sub>GS</sub> = 0 V	_	_	-10	
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 0 V	-40	_	_	V
Drain-source breakdown voltage (Note 4)	V <sub>(BR)DSX</sub>	I <sub>D</sub> = -10 mA, V <sub>GS</sub> = 10 V	-30	_	_	
Gate threshold voltage	$V_{th}$	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$	-2.0	_	-3.0	
Drain-source on-resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = -6 V, I <sub>D</sub> = -5 A	_	42	62	mΩ
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A	_	33.8	44	

Note 4: If a forward bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

## 6.2. Dynamic Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	930	_	pF
Reverse transfer capacitance	C <sub>rss</sub>		_	90	_	
Output capacitance	C <sub>oss</sub>		_	140	_	
Switching time (rise time)	t <sub>r</sub>	See Figure 6.2.1.	_	7	_	ns
Switching time (turn-on time)	t <sub>on</sub>		_	15	_	
Switching time (fall time)	t <sub>f</sub>		_	40	_	
Switching time (turn-off time)	t <sub>off</sub>			145	_	

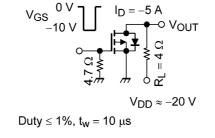


Fig. 6.2.1 Switching Time Test Circuit

## 6.3. Gate Charge Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} \approx -32 \text{ V}, V_{GS} = -10 \text{ V}, I_{D} = -10 \text{ A}$	_	19		nC
Gate-source charge	Q <sub>gs</sub>		1	13.5	1	
Gate-drain charge	$Q_{gd}$		_	5.5		

## 6.4. Source-Drain Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (DC)	(Note 5)	I <sub>DR</sub>	_	_	_	-10	Α
Reverse drain current (pulsed)	(Note 5)	I <sub>DRP</sub>	_	_	_	-20	
Diode forward voltage		$V_{DSF}$	$I_{DR}$ = -10 A, $V_{GS}$ = 0 V	_	_	1.2	V
Reverse recovery time		t <sub>rr</sub>	I <sub>DR</sub> = -10 A, V <sub>GS</sub> = 0 V	_	28	_	ns
Reverse recovery charge		Q <sub>rr</sub>	dl <sub>DR</sub> /dt = 50 A/μs	_	11	_	nC

Note 5: Ensure that the channel temperature does not exceed 175°C.



## 7. Marking (Note)

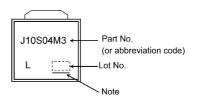


Fig. 7.1 Marking

Note: A line under a Lot No. identifies the indication of product Labels.

Not underlined: [[Pb]]/INCLUDES > MCV

Underlined: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

 ${\it Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS}$ 

compatibility of Product.

The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on

the restriction of the use of certain hazardous substances in electrical and electronic equipment.

### 8. Characteristics Curves (Note)

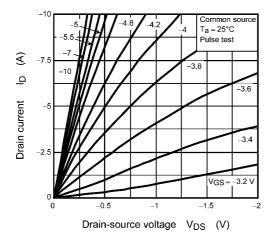


Fig. 8.1 I<sub>D</sub> - V<sub>DS</sub>

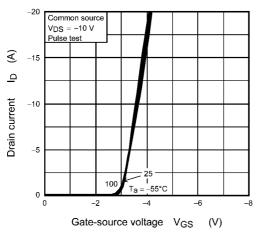


Fig. 8.3  $I_D - V_{GS}$ 

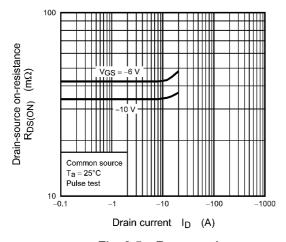


Fig. 8.5 R<sub>DS(ON)</sub> - I<sub>D</sub>

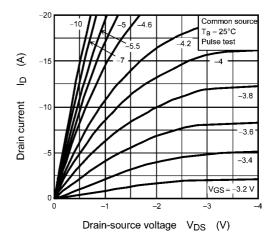


Fig. 8.2 I<sub>D</sub> - V<sub>DS</sub>

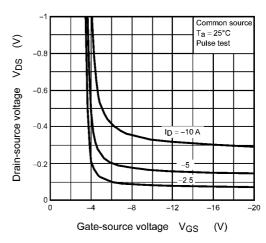


Fig. 8.4  $V_{DS}$  -  $V_{GS}$ 

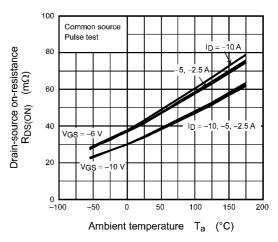


Fig. 8.6 R<sub>DS(ON)</sub> - T<sub>a</sub>

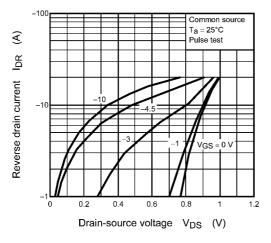


Fig. 8.7 IDR - VDS

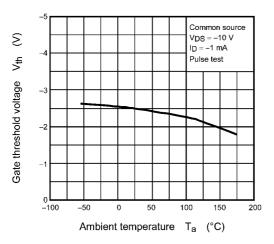


Fig. 8.9 Vth - Ta

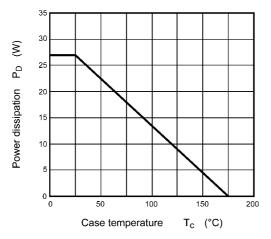


Fig. 8.11 P<sub>D</sub> - T<sub>c</sub> (Guaranteed Maximum)

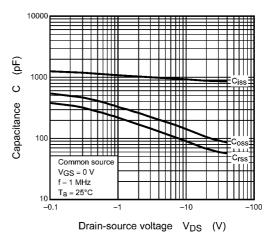


Fig. 8.8 Capacitance - V<sub>DS</sub>

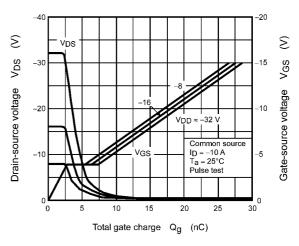


Fig. 8.10 Dynamic Input/Output Characteristics

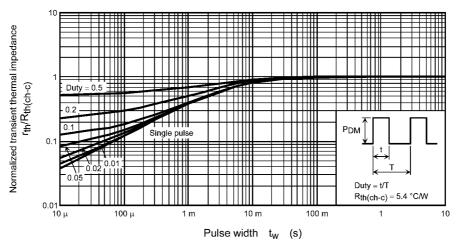


Fig. 8.12  $r_{th}/R_{th(ch-c)} - t_w$  (Guaranteed Maximum)

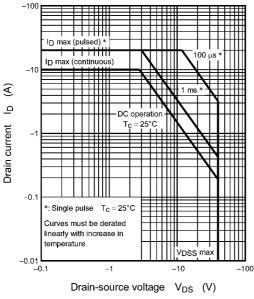


Fig. 8.13 Safe Operating Area (Guaranteed Maximum)

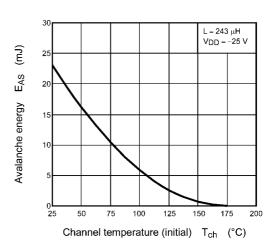


Fig. 8.14 E<sub>AS</sub> - T<sub>ch</sub> (Guaranteed Maximum)

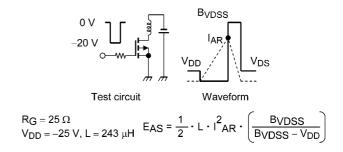


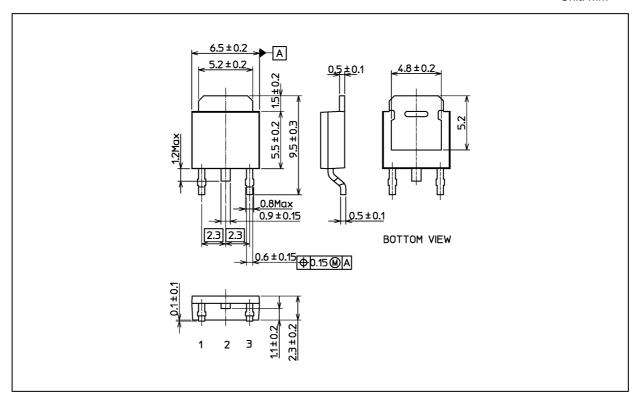
Fig. 8.15 Test Circuit/Waveform

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



## **Package Dimensions**

Unit: mm



Weight: 0.36 g (typ.)

	Package Name(s)
TOSHIBA: 2-7M1A	
Nickname: DPAK+	



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