Unit: mm

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N44FU

High Speed Switching Applications Analog Switching Applications

· Compact package suitable for high-density mounting

• Low ON-resistance : $R_{DS(ON)} = 4.0 \Omega \text{ (max) } (@V_{GS} = 4 \text{ V})$

: $R_{DS(ON)} = 7.0 \Omega \text{ (max) } (@V_{GS} = 2.5 \text{ V})$

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	30	V	
Gate-Source voltage		V_{GSS}	±20	V	
Drain current	DC	ΙD	100	mA	
	Pulse	I _{DP}	200		
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	200	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	–55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e.

report and estimated failure rate, etc).

2.1 ± 0.1 1.25 ± 0.1 0.65 1.3 ± 0.1 2.0 ± 0.2 1. SOURCE 1 4. SOURCE 2 5. GATE 2 2. GATE 1 3. DRAIN 2 6. DRAIN 1 US6 JEDEC JEITA **TOSHIBA** 2-2J1C

Weight: 6.8 mg (typ.)

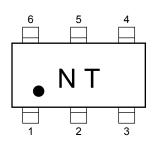
operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

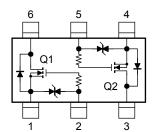
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test

Note 1: Total rating

Marking

Equivalent Circuit (top view)





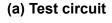
Handling Precaution

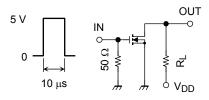
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage current		I _{GSS}	$V_{GS} = \pm 14 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА	
Drain-Source breakdown voltage		V (BR) DSS	I _D = 0.1 mA, V _{GS} = 0 V	30	_	_	V	
Drain cut-off current		I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	_	_	1	μА	
Gate threshold voltage		V _{th}	V _{DS} = 3 V, I _D = 0.1 mA	0.8	_	1.5	V	
Forward transfer admittance		Y _{fs}	V _{DS} = 3 V, I _D = 10 mA	25	_	_	mS	
Drain-Source ON resistance		R _{DS} (ON)	I _D = 10 mA, V _{GS} = 4 V	_	2.2	4.0	Ω	
			I _D = 10 mA, V _{GS} = 2.5 V	_	4.0	7.0	7.7	
Input capacitance		C _{iss}		_	8.5	_	pF	
Reverse transfer capacitance		C _{rss}	V _{DS} = 3 V, V _{GS} = 0 V, f = 1 MHz	_	5.3	_		
Output capacitance		Coss		_	9.4	_		
Switching time	Turn-on time	t _{on}	V _{DD} = 5 V, I _D = 10 mA,	_	50	_	ns	
	Turn-off time	t _{off}	V _{GS} = 0 to 5 V	_	200	_		

Switching Time Test Circuit

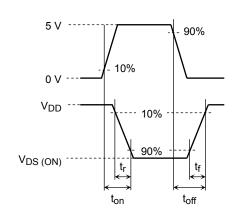




$$\begin{split} &V_{DD}=5 \text{ V}\\ &D.U.\leq 1\%\\ &V_{IN}\text{: }t_{f},\,t_{f}<5 \text{ ns}\\ &(Z_{out}=50 \text{ }\Omega)\\ &\text{Common Source}\\ &\text{Ta}=25^{\circ}\text{C} \end{split}$$

(b) V_{IN}

(c) Vout



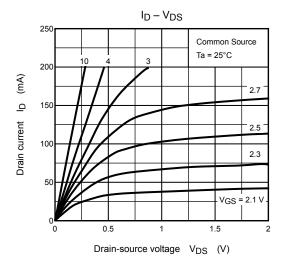
Precaution

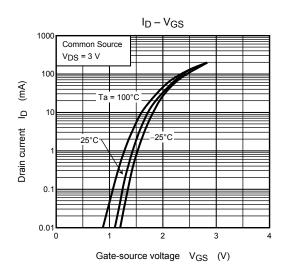
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.1mA for the SSM6N44FU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

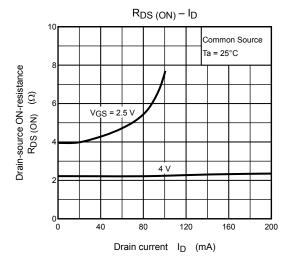
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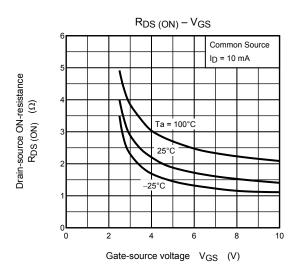
Take this into consideration when using the device.

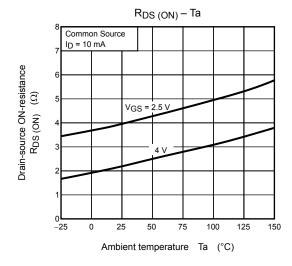
(Q1, Q2 Common)

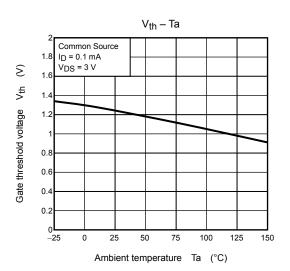




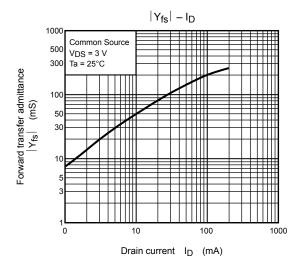


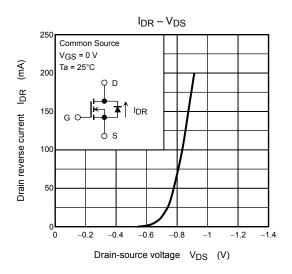


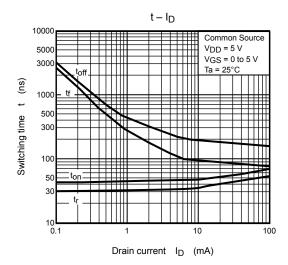


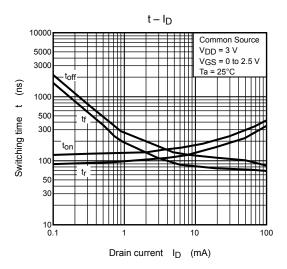


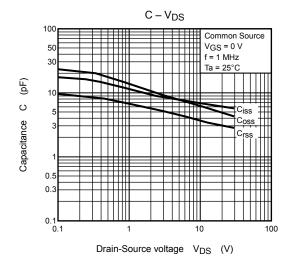
(Q1, Q2 Common)

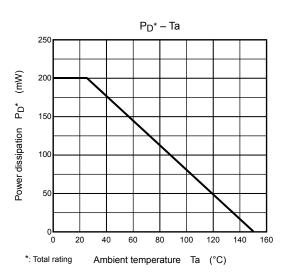












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