Unit: mm

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM6N44FE

High Speed Switching Applications Analog Switching Applications

Compact package suitable for high-density mounting

: $R_{DS(ON)}$ = 4.0 Ω (max) (@V_{GS} = 4 V) : $R_{DS(ON)}$ = 7.0 Ω (max) (@V_{GS} = 2.5 V) Low ON-resistance

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	30	V	
Gate-Source voltage		V_{GSS}	±20	٧	
Drain current	DC	ΙD	100	mA	
	Pulse	I _{DP}	200		
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling

Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 0.135 \text{ mm}^2 \times 6)$

1.6±0.05 1.2±0.05 $.6\pm0.05$ 1.0 ± 0.05 5 1 Source1 4.Source2 2.Gate1 5.Gate2 3.Drain2 6.Drain1 ES₆ **JEDEC** JEITA

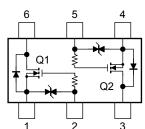
2-2N1D

Weight: 3 mg (typ.)

TOSHIBA

Marking

Equivalent Circuit (top view)



Handling Precaution

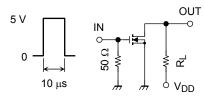
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{GS} = \pm 14 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μА
Drain-Source breakdown voltage		V (BR) DSS	I _D = 0.1 mA, V _{GS} = 0 V	30	_	_	V
Drain cut-off current		I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	_	_	1	μА
Gate threshold voltage		V _{th}	$V_{DS} = 3 \text{ V}, I_{D} = 0.1 \text{ mA}$	0.8	_	1.5	V
Forward transfer admittance		Y _{fs}	V _{DS} = 3 V, I _D = 10 mA	25	_	_	mS
Drain-Source ON resistance		R _{DS} (ON)	I _D = 10 mA, V _{GS} = 4 V	_	2.2	4.0	Ω
			I _D = 10 mA, V _{GS} = 2.5 V	_	4.0	7.0	
Input capacitance		C _{iss}		_	8.5	_	pF
Reverse transfer capacitance		C _{rss}	V _{DS} = 3 V, V _{GS} = 0 V, f = 1 MHz	_	5.3	_	
Output capacitance		Coss		_	9.4	_	
Switching time	Turn-on time	t _{on}	V _{DD} = 5 V, I _D = 10 mA,	_	50	_	20
	Turn-off time	t _{off}	V _{GS} = 0 to 5 V	_	200	_	ns

Switching Time Test Circuit

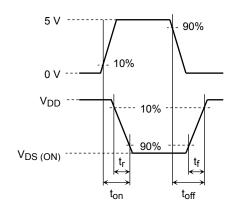




$$\begin{split} &V_{DD}=5 \text{ V}\\ &D.U.\leq 1\%\\ &V_{IN}\text{: }t_{f},\,t_{f}<5 \text{ ns}\\ &(Z_{out}=50 \text{ }\Omega)\\ &\text{Common Source}\\ &\text{Ta}=25^{\circ}\text{C} \end{split}$$

(b) V_{IN}

(c) Vout



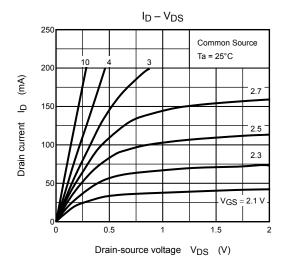
Precaution

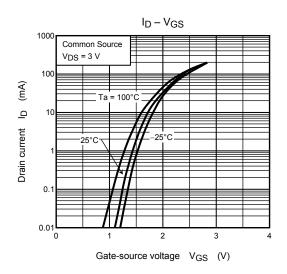
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.1mA for the SSM6N44FE). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

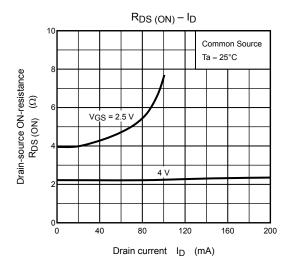
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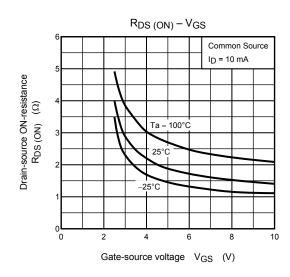
Take this into consideration when using the device

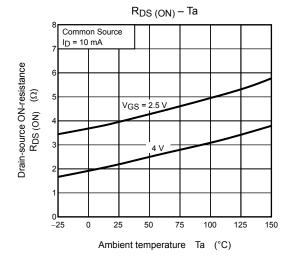
(Q1, Q2 Common)

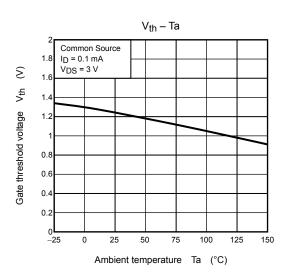






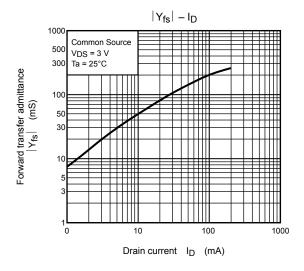


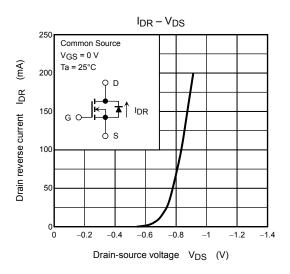


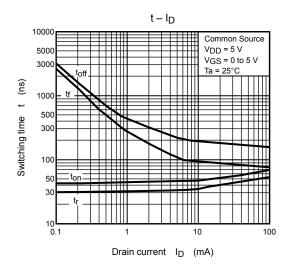


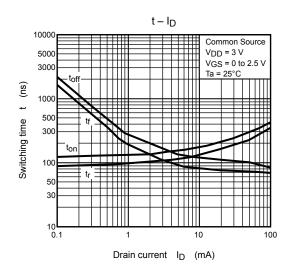
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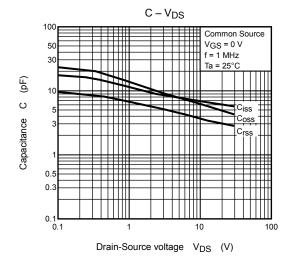
(Q1, Q2 Common)

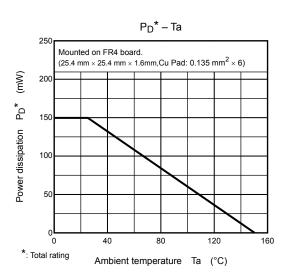












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