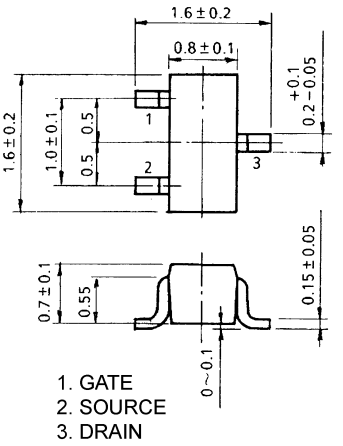
TOSHIBA Field-Effect Transistor Silicon N Channel MOS Type

SSM3K43FS

○ High-Speed Switching Applications

- 1.5-V drive
- Low ON-resistance : R_{on} = 1.52 Ω (max) (@V_{GS} = 1.5V)
  : R_{on} = 1.14 Ω (max) (@V_{GS} = 1.8V)
  : R_{on} = 0.85 Ω (max) (@V_{GS} = 2.5V)
  : R_{on} = 0.66 Ω (max) (@V_{GS} = 4.5V)
  : R_{on} = 0.63 Ω (max) (@V_{GS} = 5.0V)

Unit: mm



SSM	
JEDEC	—
JEITA	—
TOSHIBA	2-2H1B

Weight: 2.4mg (typ.)

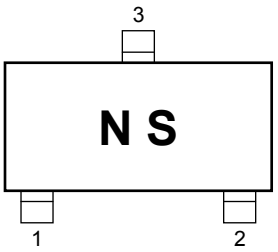
Absolute Maximum Ratings (Ta = 25 °C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	20	V
Gate-source voltage		V_{GSS}	± 10	V
Drain current	DC	I_D	500	mA
	Pulse	I_{DP}	1000	
Drain power dissipation		P_D (Note1)	150	mW
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

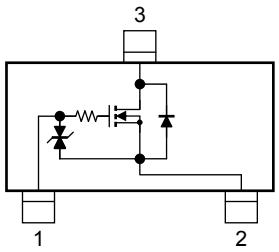
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board. (25.4 mm × 25.4 mm × 1.6 mm, 0.36 mm^2 ×3)

Marking



Equivalent Circuit (top view)



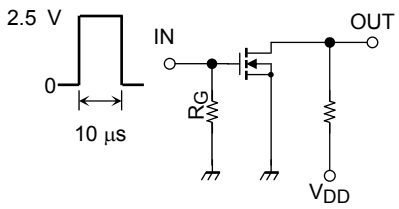
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 1 mA, V_{GS} = 0	20	—	—	V
		$V_{(BR)\ DSX}$	I_D = 1 mA, V_{GS} = - 10 V	12	—	—	
Drain cutoff current		I_{DSS}	V_{DS} = 20 V, V_{GS} = 0	—	—	1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0	—	—	±1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3 V, I_D = 1 mA	0.35	—	1.0	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3 V, I_D = 200 mA (Note2)	420	840	—	mS
Drain-source ON-resistance		$R_{DS\ (ON)}$	I_D = 200 mA, V_{GS} = 5.0 V (Note2)	—	0.46	0.63	Ω
			I_D = 200 mA, V_{GS} = 4.5 V (Note2)	—	0.51	0.66	
			I_D = 200 mA, V_{GS} = 2.5 V (Note2)	—	0.66	0.85	
			I_D = 100 mA, V_{GS} = 1.8 V (Note2)	—	0.81	1.14	
			I_D = 50 mA, V_{GS} = 1.5 V (Note2)	—	0.95	1.52	
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	46	—	pF
Output capacitance		C_{oss}		—	10.8	—	
Reverse transfer capacitance		C_{rss}		—	7.3	—	
Total Gate Charge		Q_g	V_{DS} = 10 V, I_D = 0.5 A V_{GS} = 4.0 V	—	1.23	—	nC
Gate−Source Charge		Q_{gs}		—	0.60	—	
Gate−Drain Charge		Q_{gd}		—	0.63	—	
Switching time	Turn-on time	t_{on}	V_{DD} = 10 V, I_D = 200 mA V_{GS} = 0 to 2.5 V, R_G = 50 Ω	—	30	—	ns
	Turn-off time	t_{off}		—	75	—	
Drain-source forward voltage		V_{DSF}	I_D = -0.5 A, V_{GS} = 0 V (Note2)	—	-0.88	-1.2	V

Note2: Pulse test

Switching Time Test Circuit

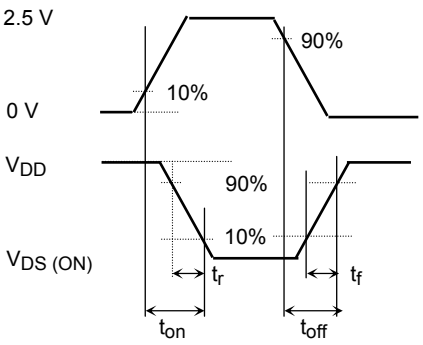
(a) Test Circuit



V_{DD} = 10 V
R_G = 50 Ω
D.U. ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}



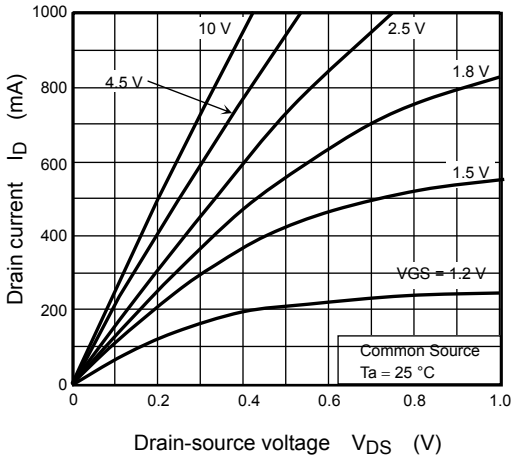
Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below (1 mA for the SSM3K43FS). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th}, and $V_{GS(off)}$ must be lower than V_{th}. This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.
Take this into consideration when using the device.

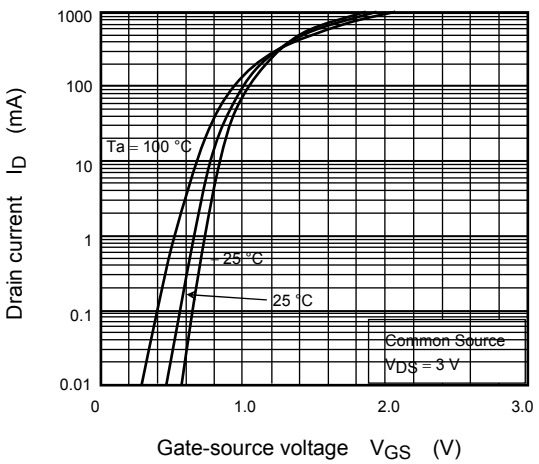
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

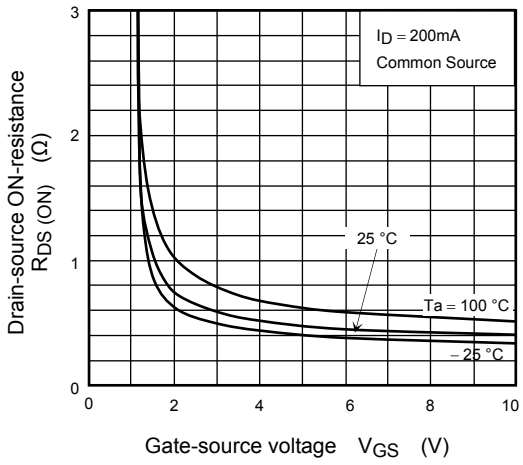
$I_D - V_{DS}$



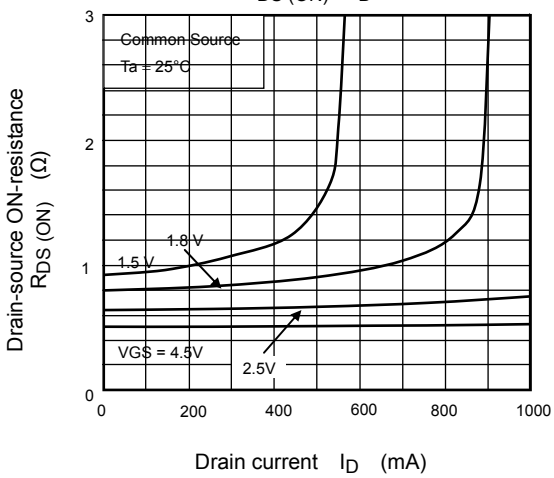
$I_D - V_{GS}$



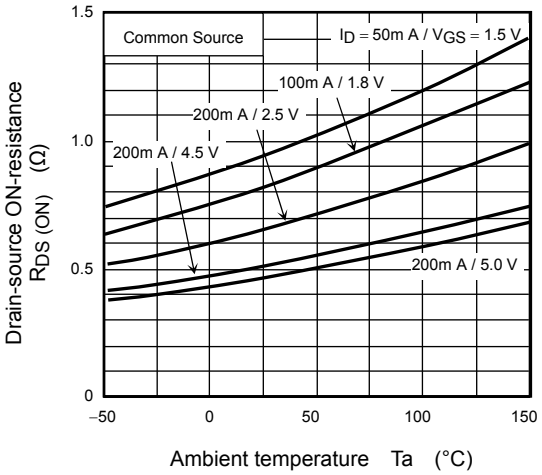
$R_{DS\ (ON)} - V_{GS}$



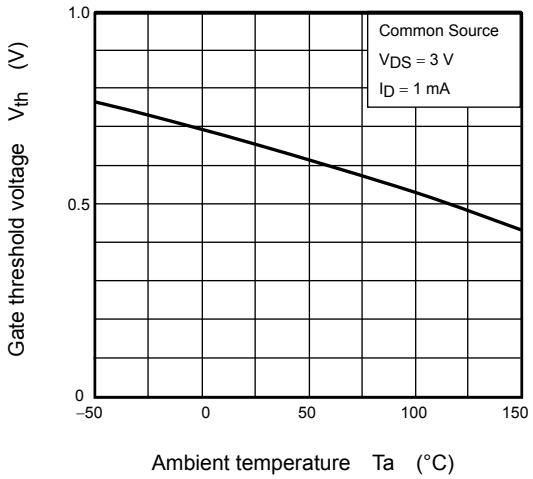
$R_{DS\ (ON)} - I_D$

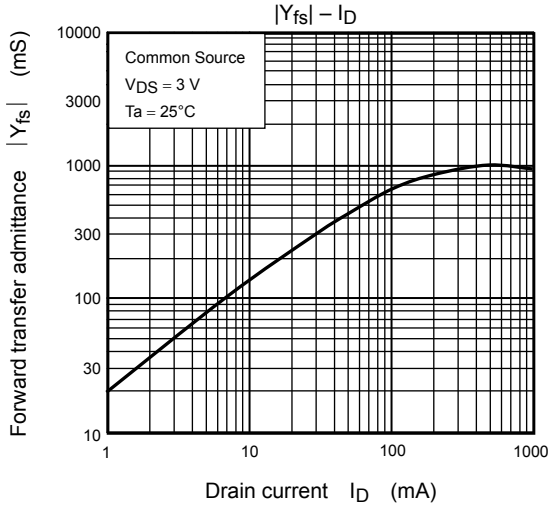


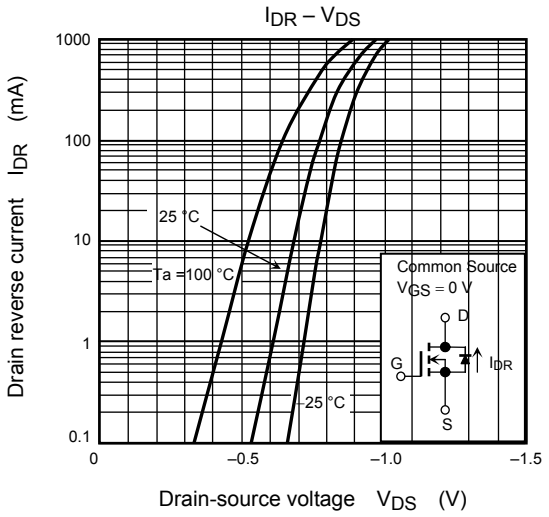
$R_{DS\ (ON)} - Ta$

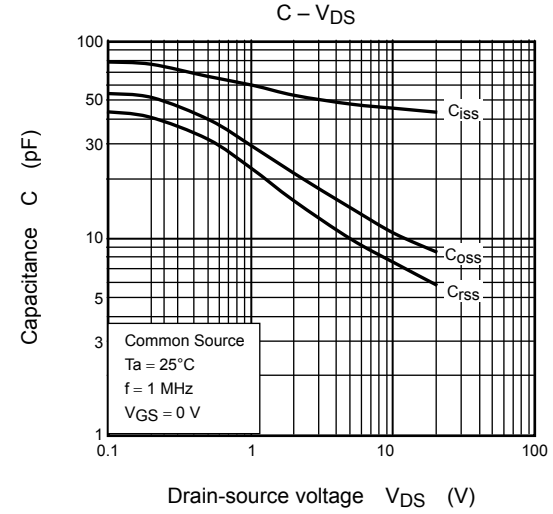


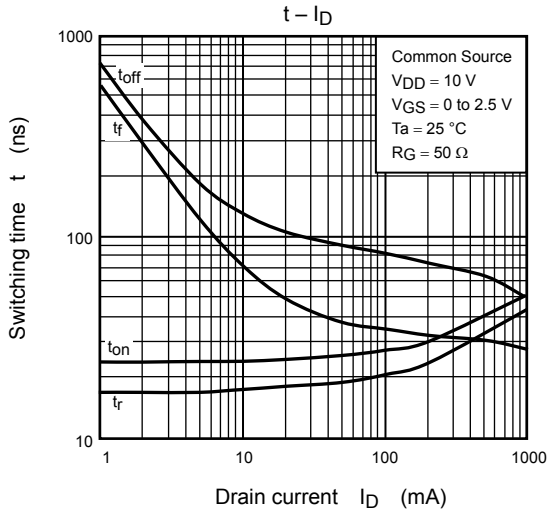
$V_{th} - Ta$

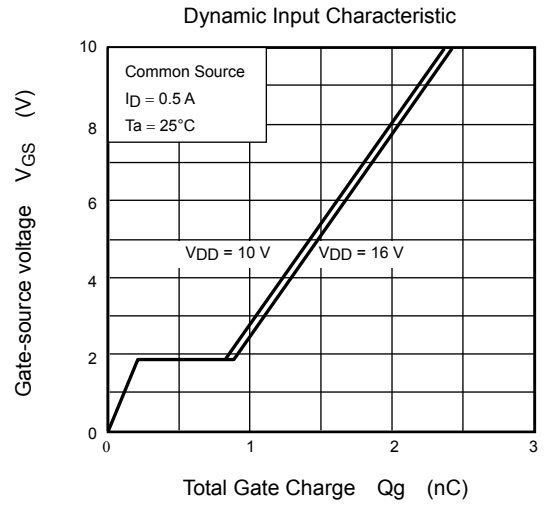


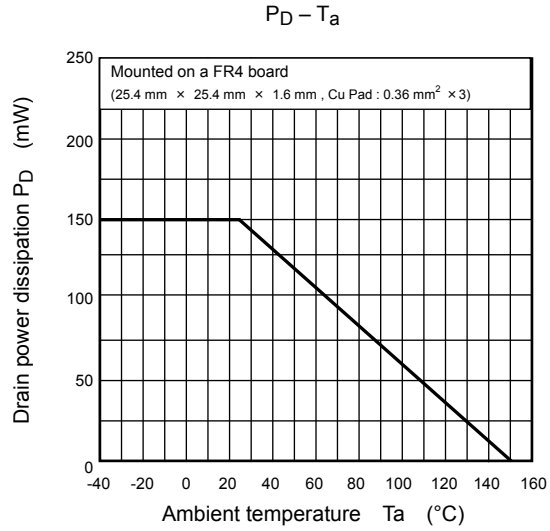

|Yfs| – ID
Common Source
VDS = 3 V
Ta = 25°C
Forward transfer admittance |Yfs| (mS)
Drain current ID (mA)
10000
3000
1000
300
100
30
10
1
10
100
1000


IDR – VDS
Drain reverse current IDR (mA)
Drain-source voltage VDS (V)
25 °C
Ta = 100 °C
25 °C
Common Source
VGS = 0 V
D
G
S
IDR
1000
100
10
1
0.1
0
–0.5
–1.0
–1.5


C – VDS
Capacitance C (pF)
Drain-source voltage VDS (V)
Ciss
Coss
Crss
Common Source
Ta = 25°C
f = 1 MHz
VGS = 0 V
100
50
30
10
5
3
1
0.1
1
10
100


t – ID
Switching time t (ns)
Drain current ID (mA)
toff
tf
ton
tr
Common Source
VDD = 10 V
VGS = 0 to 2.5 V
Ta = 25 °C
RG = 50 Ω
1000
100
10
1
10
100
1000


Dynamic Input Characteristic
Gate-source voltage VGS (V)
Total Gate Charge Qg (nC)
Common Source
ID = 0.5 A
Ta = 25°C
VDD = 10 V
VDD = 16 V
10
8
6
4
2
0
0
1
2
3


PD – Ta
Drain power dissipation PD (mW)
Ambient temperature Ta (°C)
Mounted on a FR4 board
(25.4 mm × 25.4 mm × 1.6 mm , Cu Pad : 0.36 mm2 ×3)
250
200
150
100
50
0
-40
-20
0
20
40
60
80
100
120
140
160

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