

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

# SSM3K37CT

- High Speed Switching Applications
- Analog Switch Applications

- 1.5Vdrive
- Low ON-resistance
  - $R_{DS(ON)} = 5.60 \Omega$  (max) (@ $V_{GS} = 1.5 V$ )
  - $R_{DS(ON)} = 4.05 \Omega$  (max) (@ $V_{GS} = 1.8 V$ )
  - $R_{DS(ON)} = 3.02 \Omega$  (max) (@ $V_{GS} = 2.5 V$ )
  - $R_{DS(ON)} = 2.20 \Omega$  (max) (@ $V_{GS} = 4.5 V$ )

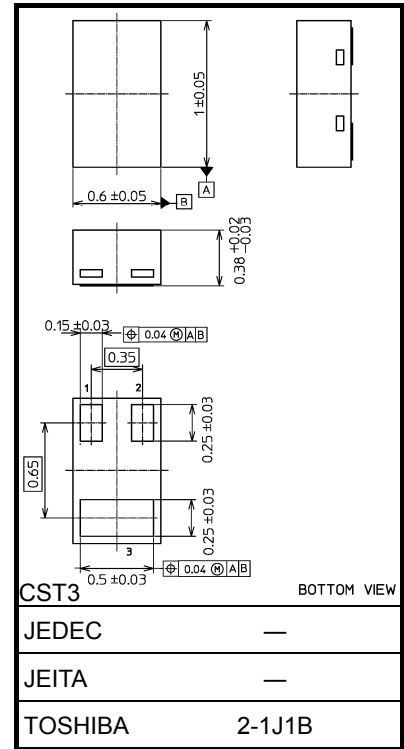
## Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		$V_{DSS}$	20	V
Gate-Source voltage		$V_{GSS}$	$\pm 10$	V
Drain current	DC	$I_D$	200	mA
	Pulse	$I_{DP}$	400	
Power dissipation		$P_D$ (Note1)	100	mW
Channel temperature		$T_{ch}$	150	°C
Storage temperature range		$T_{stg}$	-55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

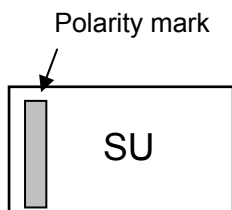
Note 1: Mounted on FR4 board  
(10 mm × 10 mm × 1.0 mm, Cu Pad: 100 mm<sup>2</sup>)

Unit : mm

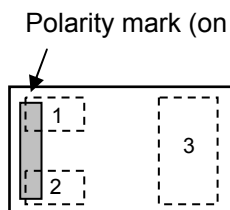


Weight: 0.75mg(typ.)

### Marking(top view)

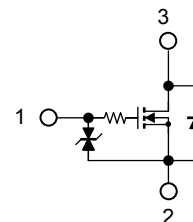


### Pin Condition (top view)



1. Gate
  2. Source
  3. Drain
- \*Electrodes: On the bottom

### Equivalent Circuit



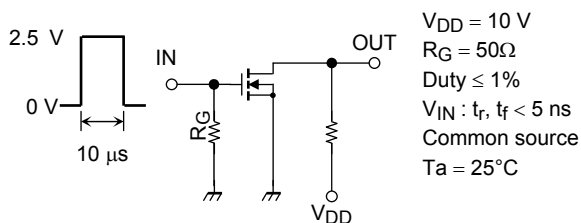
## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	20	—	—	V
	$V_{(BR)DSX}$	$I_D = 1 \text{ mA}, V_{GS} = -10 \text{ V}$	12	—	—	
Drain cut-off current	$I_{DSS}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$	0.35	—	1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3 \text{ V}, I_D = 100 \text{ mA}$ (Note2)	0.14	0.28	—	S
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = 100 \text{ mA}, V_{GS} = 4.5 \text{ V}$ (Note2)	—	1.65	2.20	$\Omega$
		$I_D = 50 \text{ mA}, V_{GS} = 2.5 \text{ V}$ (Note2)	—	2.16	3.02	
		$I_D = 20 \text{ mA}, V_{GS} = 1.8 \text{ V}$ (Note2)	—	2.66	4.05	
		$I_D = 10 \text{ mA}, V_{GS} = 1.5 \text{ V}$ (Note2)	—	3.07	5.60	
Input capacitance	$C_{iss}$	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	—	12	—	pF
Output capacitance	$C_{oss}$		—	5.5	—	
Reverse transfer capacitance	$C_{rss}$		—	4.1	—	
Switching time	Turn-on time	$t_{on}$	$V_{DD} = 10 \text{ V}, I_D = 100 \text{ mA}$		—	ns
	Turn-off time	$t_{off}$	$V_{GS} = 0 \text{ to } 2.5 \text{ V}, R_G = 50 \Omega$		—	
Drain-Source forward voltage	$V_{DSF}$	$I_D = -200 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note2)	—	-0.89	-1.2	V

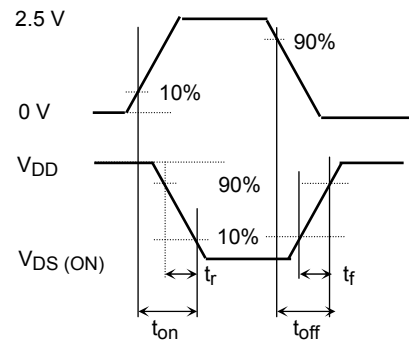
Note2: Pulse test

## Switching Time Test Circuit

(a) Test Circuit



(b)  $V_{IN}$



(c)  $V_{OUT}$

## Precaution

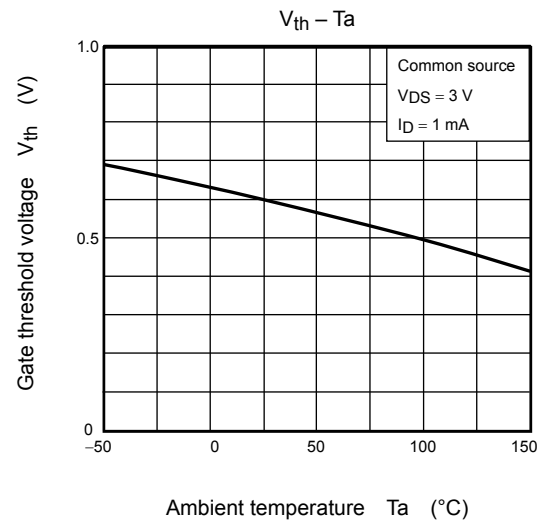
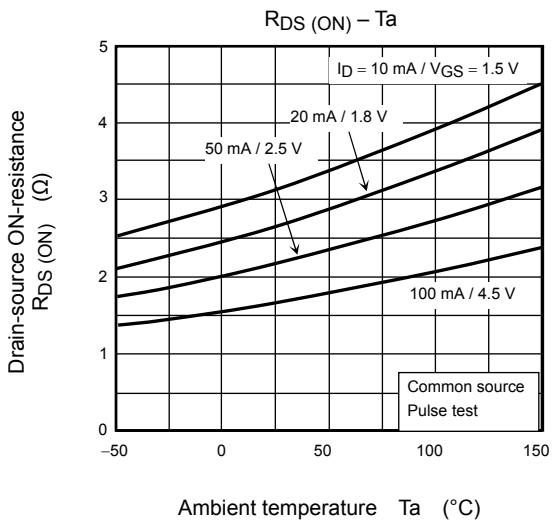
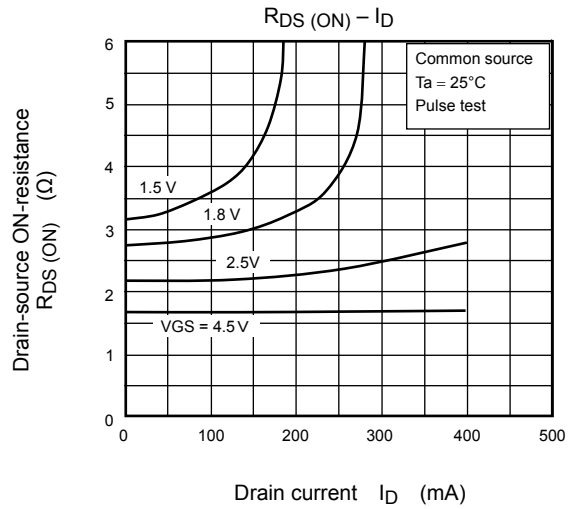
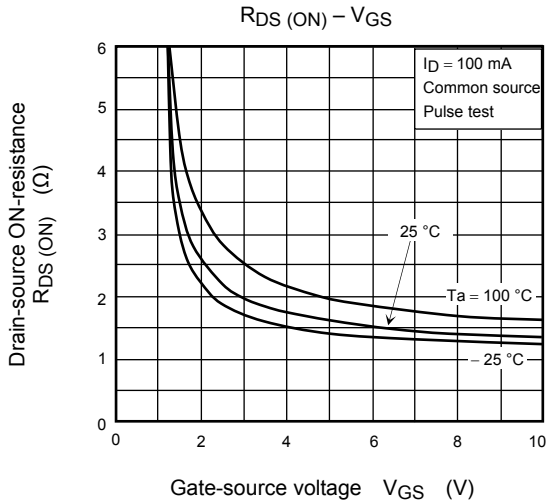
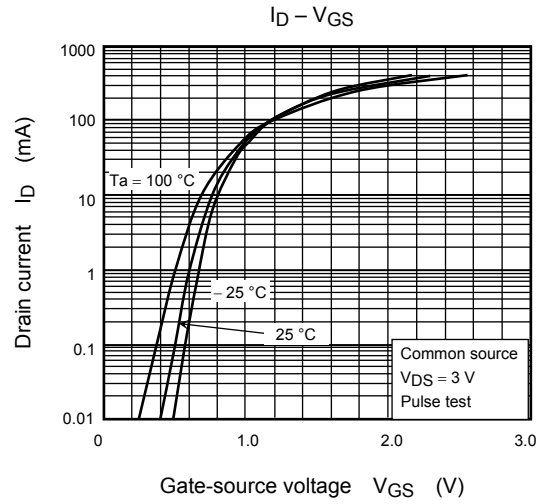
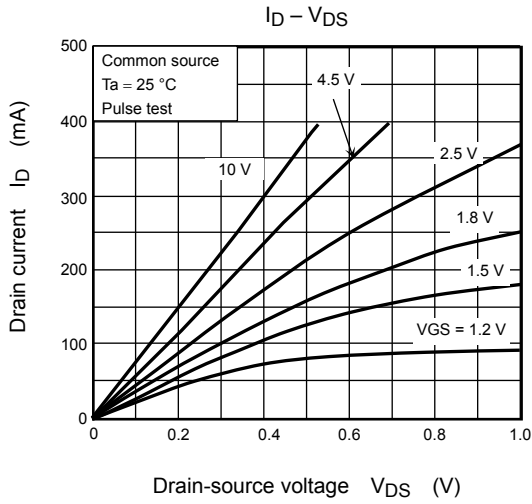
Let  $V_{th}$  be the voltage applied between gate and source that causes the drain current ( $I_D$ ) to be low (1mA for the SSM3K37CT). Then, for normal switching operation,  $V_{GS(on)}$  must be higher than  $V_{th}$ , and  $V_{GS(off)}$  must be lower than  $V_{th}$ . This relationship can be expressed as:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ .

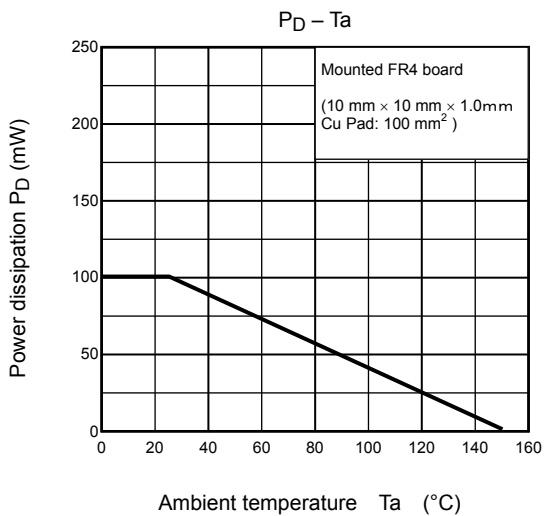
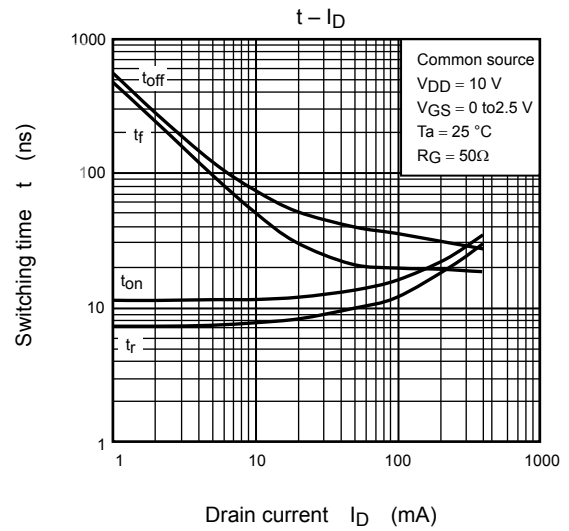
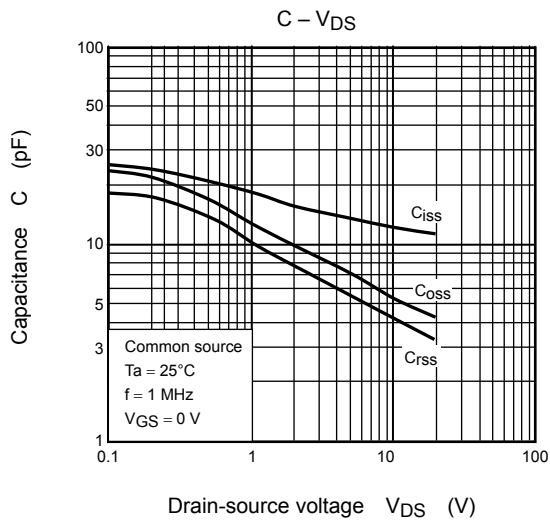
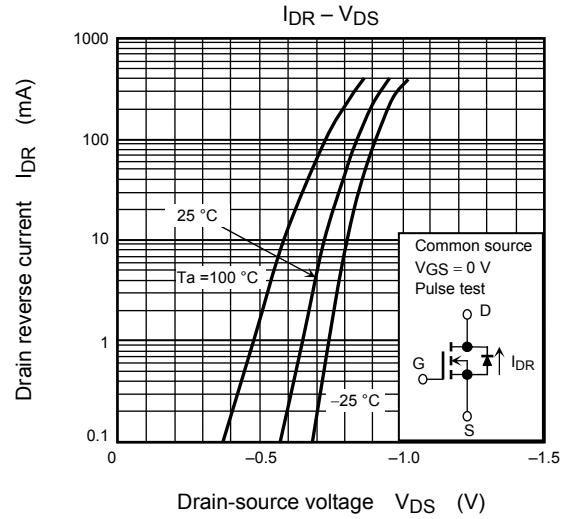
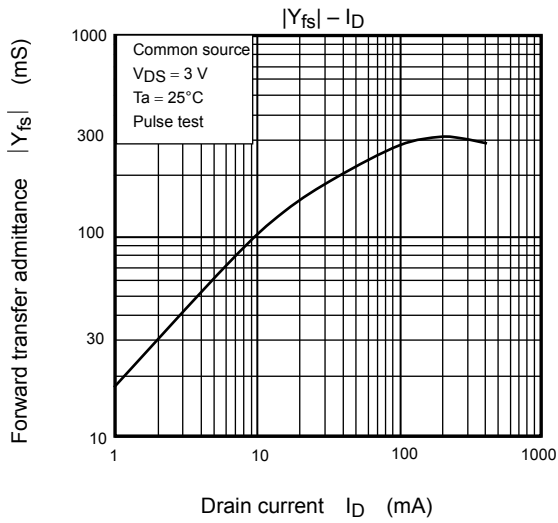
Take this into consideration when using the device.

## Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance  $R_{th(ch-a)}$  and power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration





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