TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

# SSM3K01F

## **High Speed Switching Applications**

Unit: mm

- Small package
- Low on resistance: Ron = 120 m $\Omega$  (max) (VGS = 4 V)

: Ron = 150 m $\Omega$  (max) (VGS = 2.5 V)

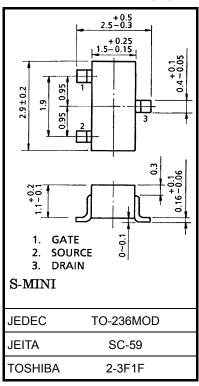
• Low gate threshold voltage:  $V_{th} = 0.6 \sim 1.1 \text{ V (V}_{DS} = 3 \text{ V, I}_{D} = 0.1 \text{ mA})$ 

## **Absolute Maximum Ratings (Ta = 25°C)**

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		$V_{DS}$	30	V	
Gate-source voltage		V <sub>GSS</sub>	±10	V	
Drain current	DC	I <sub>D</sub>	1.3	Α	
	Pulse	I <sub>DP</sub>	2.6		
Drain power dissipation		P <sub>D</sub>	200	mW	
Channel temperature		T <sub>ch</sub>	150	°C	
Storage temperature range		T <sub>stg</sub>	-55~150	°C	

Note:

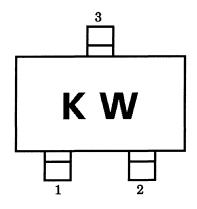
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.



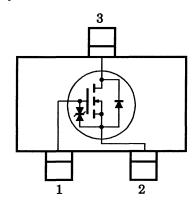
Weight: 0.012 g (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

#### Marking



#### **Equivalent Circuit**



# **Handling Precaution**

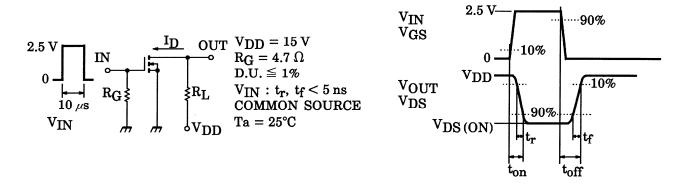
When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

# **Electrical Characteristics (Ta = 25°C)**

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I <sub>GSS</sub>	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$	_	_	±5	μА
Drain-source breakdown voltage		V (BR) DSS	$I_D = 1$ mA, $V_{GS} = 0$	30	_	_	V
Drain cut-off current		I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0$	_	_	1	μА
Gate threshold vo	Itage	$V_{th}$	$V_{DS} = 3 \text{ V}, I_D = 0.1 \text{ mA}$	0.6	_	1.1	V
Forward transfer a	admittance	Y <sub>fs</sub>	$V_{DS} = 3 \text{ V}, I_D = 0.65 \text{ A}$ (Note	2.0	_	_	S
Drain-source ON resistance		R <sub>DS (ON)</sub>	$I_D = 0.65 \text{ A}, V_{GS} = 4 \text{ V}$ (Note	) —	85	120	mΩ
			$I_D = 0.65 \text{ A}, V_{GS} = 2.5 \text{ V}$ (Note	) —	115	150	
Input capacitance		C <sub>iss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		152	_	pF
Reverse transfer capacitance		C <sub>rss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		41	_	pF
Output capacitance		C <sub>oss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		102	_	pF
Switching time	Turn-on time	t <sub>on</sub>	$V_{DD} = 15 \text{ V}, \ I_D = 0.5 \text{ A}, \ V_{GS} = 02.5 \text{ V}, \ R_G = 4.7 \ \Omega$	_	45	_	- ns
	Turn-off time	t <sub>off</sub>		_	69	_	

Note: Pulse test

# **Switching Time Test Circuit**

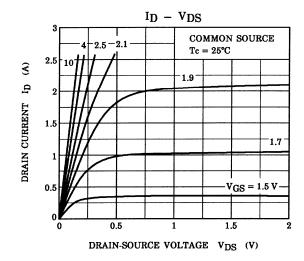


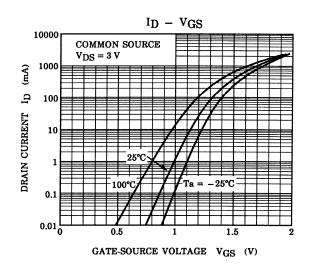
#### **Precaution**

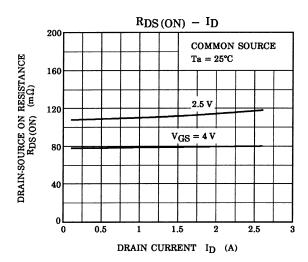
 $V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D = 100~\mu A$  for this product. For normal switching operation,  $V_{GS}$  (ON) requires higher voltage than  $V_{th}$  and  $V_{GS}$  (off) requires lower voltage than  $V_{th}$ .

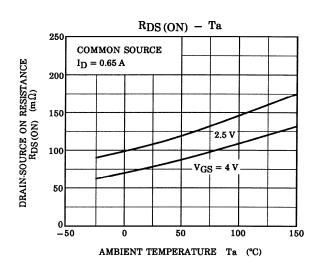
(Relationship can be established as follows:  $V_{GS}$  (off)  $< V_{th} < V_{GS}$  (ON))

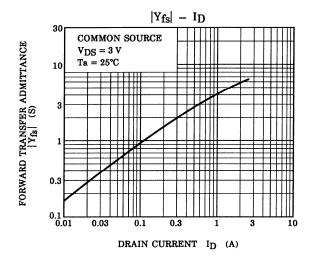
Please take this into consideration for using the device.

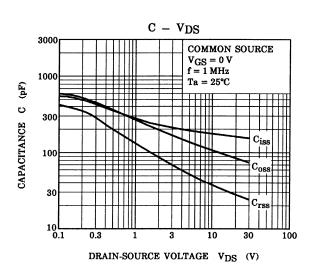




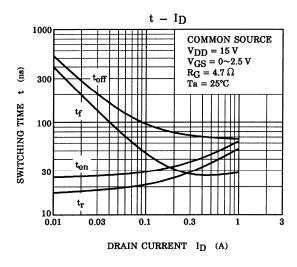


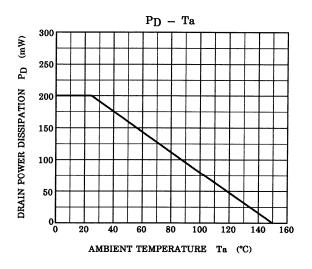






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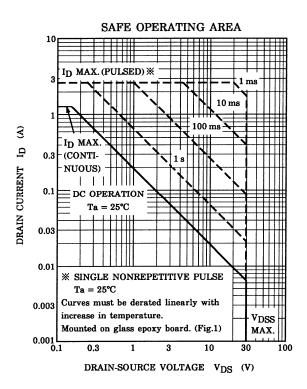




Figure 1 25.4 mm  $\times$  25.4 mm  $\times$  1.6 t (a Cu pad of 0.8 mm<sup>2</sup> area)

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