

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

## SSM3J09FU

Management Switch  
High Speed Switching Applications

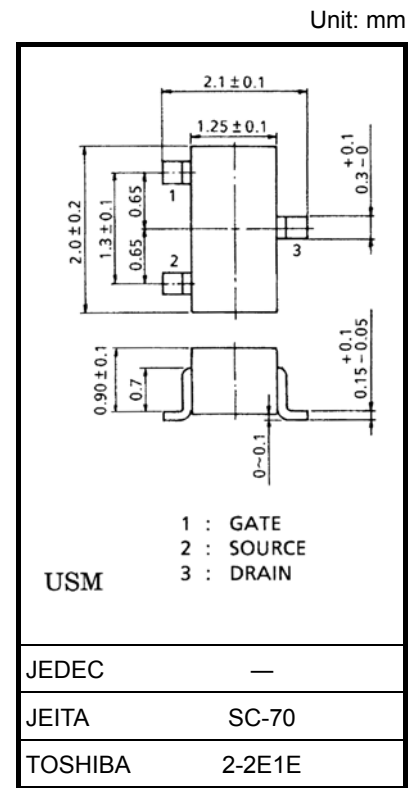
- Small package
- Low on resistance:  $R_{on} = 2.7 \Omega$  (max) (@ $V_{GS} = -10 V$ )  
:  $R_{on} = 4.2 \Omega$  (max) (@ $V_{GS} = -4 V$ )

### Absolute Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Drain-Source voltage	$V_{DS}$	-30	V
Gate-Source voltage	$V_{GSS}$	±20	V
Drain current	DC	$I_D$	-200
	Pulse	$I_{DP}$	-400
Drain power dissipation (Ta = 25°C)	$P_D$ (Note 1)	150	mW
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55~150	°C

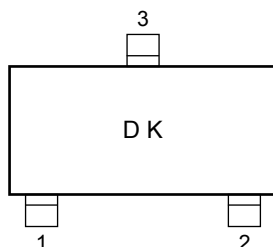
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board  
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.6 mm<sup>2</sup> × 3) Figure 1.



Weight: 0.006 g (typ.)

### Marking



### Equivalent Circuit (top view)

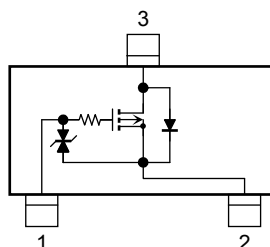
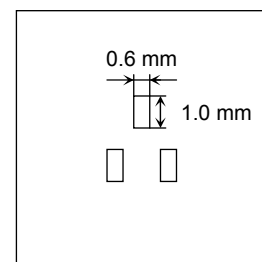


Figure 1: 25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.6 mm<sup>2</sup> × 3



### Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

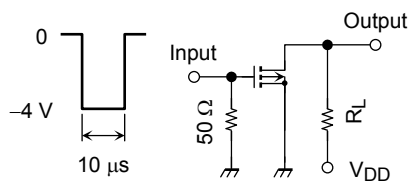
## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0$	—	—	$\pm 1$	$\mu\text{A}$
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1\text{ mA}, V_{GS} = 0$	-30	—	—	V
Drain cut-off current	$I_{DSS}$	$V_{DS} = -30\text{ V}, V_{GS} = 0$	—	—	-1	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = -5\text{ V}, I_D = -0.1\text{ mA}$	-1.1	—	-1.8	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -5\text{ V}, I_D = -100\text{ mA}$ (Note2)	115	—	—	mS
Drain-Source ON resistance	$R_{DS(ON)}$	$I_D = -100\text{ mA}, V_{GS} = -10\text{ V}$ (Note2)	—	2.1	2.7	$\Omega$
		$I_D = -100\text{ mA}, V_{GS} = -4\text{ V}$ (Note2)	—	3.3	4.2	
		$I_D = -100\text{ mA}, V_{GS} = -3.3\text{ V}$ (Note2)	—	4.0	6.0	
Input capacitance	$C_{iss}$	$V_{DS} = -5\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	22	—	pF
Reverse transfer capacitance	$C_{rss}$	$V_{DS} = -5\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	5	—	pF
Output capacitance	$C_{oss}$	$V_{DS} = -5\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	14	—	pF
Switching time	Turn-on time	$t_{on}$	—	85	—	ns
	Turn-off time	$t_{off}$				

Note 2: Pulse test

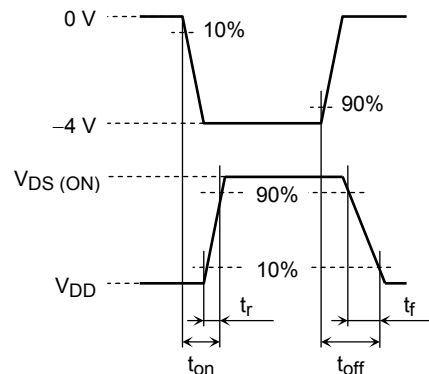
## Switching Time Test Circuit

### (a) Test circuit



$V_{DD} = -5\text{ V}$   
 D.U.  $\leq 1\%$   
 Input:  $t_r, t_f < 5\text{ ns}$   
 ( $Z_{out} = 50\ \Omega$ )  
 Common Source  
 Ta = 25°C

### (b) $V_{IN}$



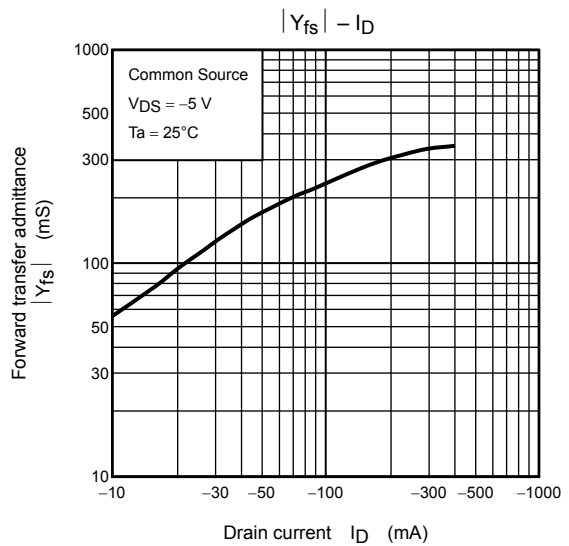
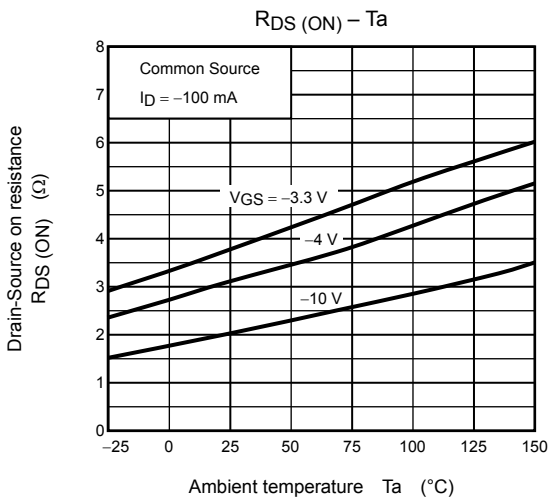
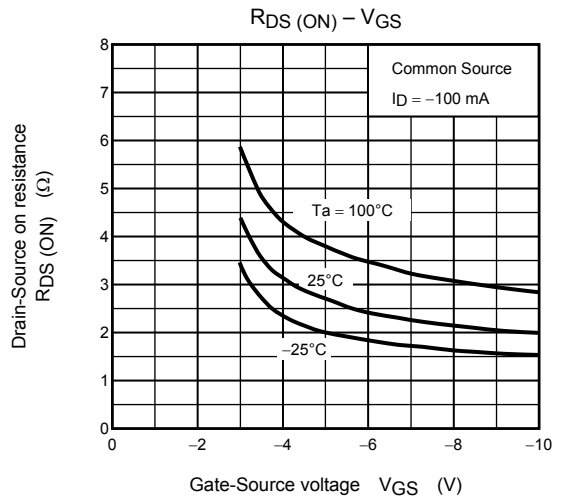
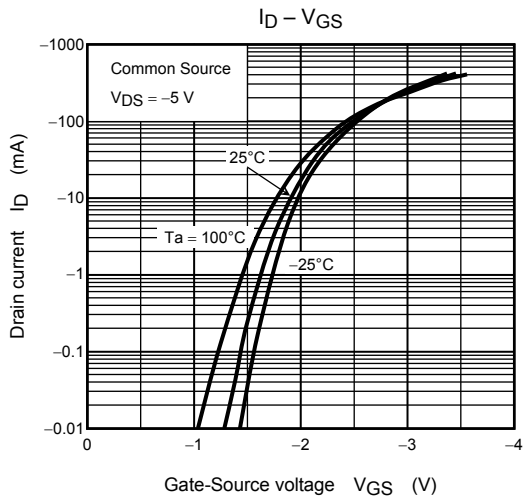
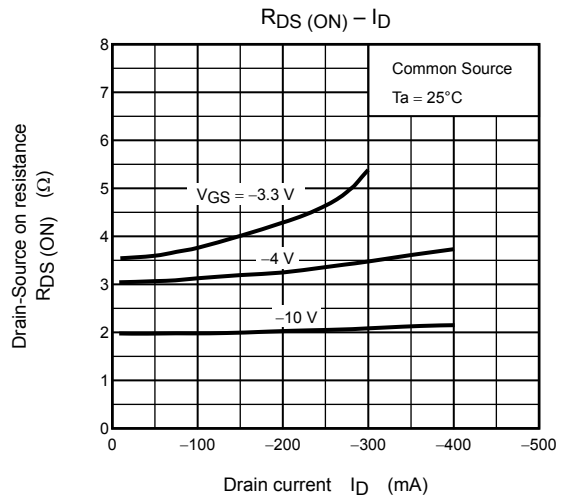
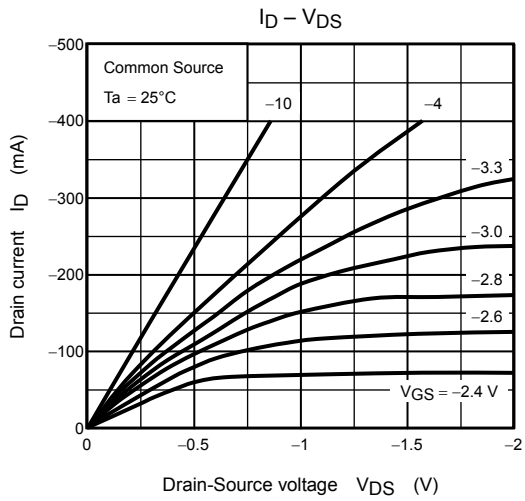
### (c) $V_{OUT}$

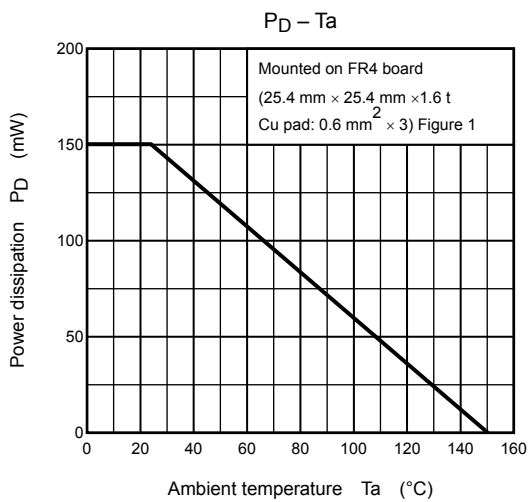
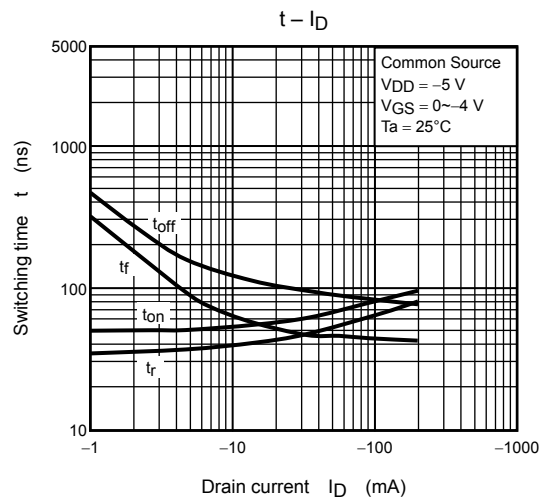
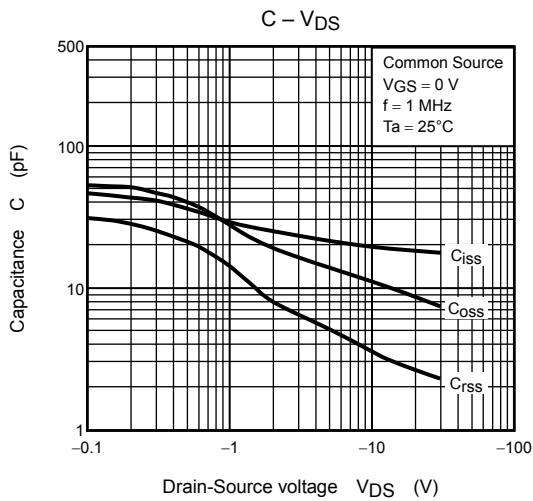
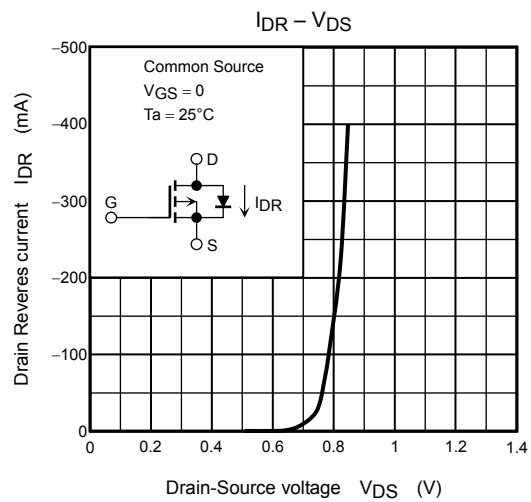
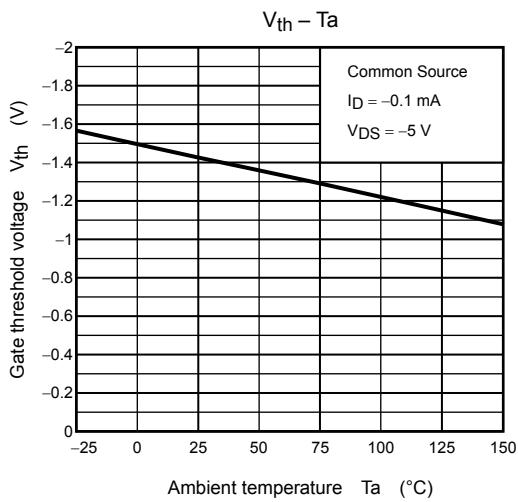
## Precaution

$V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D = -100\ \mu\text{A}$  for this product. For normal switching operation,  $V_{GS(ON)}$  requires higher voltage than  $V_{th}$  and  $V_{GS(OFF)}$  requires lower voltage than  $V_{th}$ .

(relationship can be established as follows:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ )

Please take this into consideration for using the device.





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