DSKTJ05

Silicon N-channel Junction FET

For impedance conversion in low frequency

■ Features

- High speed stability time
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

■ Packaging

Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

■ Package

- Code
  TSSSMini3-F2-B
- Pin Name
  1: Drain
  2: Source
  3: Gate

■ Marking Symbol: 9

■ Absolute Maximum Ratings $T_a = 25°C$

Parameter	Symbol	Rating	Unit
Drain-source voltage (Gate open)	V_{DSO}	20	V
Drain-gate voltage (Souece open)	V_{DGO}	20	V
Drain-source current (Gate open)	I_{DSO}	2	mA
Drain-gate current (Souece open)	I_{DGO}	2	mA
Power dissipation	P_D	100	mW
Operating ambient temperature	T_{opr}	–20 to +80	°C
Storage temperature	T_{stg}	–55 to +150	°C

■ Electrical Characteristics $T_a = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain current*1	I_D	V_{DS} = 2.0 V, R_d = 2.2 kΩ ± 1%	100		320	μA
Drain-source cutoff current *2	I_{DSS}	V_{DS} = 2.0 V, R_d = 2.2 kΩ ± 1%, V_{GS} = 0	110		310	μA
Forward transfer admittance	$\|Y_{fs}\|$	V_D = 2.0 V, V_{GS} = 0, f = 1 MHz	660	1 500		μS
Noise voltage *3	NV	V_D = 2.0 V, R_d = 2.2 kΩ ± 1%, C_O = 5 pF, A-curve			8	μV
Voltage gain	G_{V1}	V_D = 2.0 V, R_d = 2.2 kΩ ± 1%, C_O = 5 pF, eG = 10 mV, f = 1 kHz	–5.0	–1.0		dB
	G_{V2}	V_D = 1.5 V, R_d = 2.2 kΩ ± 1%, C_O = 5 pF, eG = 10 mV, f = 1 kHz	–7.0	–1.5		dB
	$\Delta\|G_V . f\|$ *4	V_D = 2.0 V, R_d = 2.2 kΩ ± 1%, C_O = 5 pF, eG = 10 mV, f = 1 kHz to 70 Hz		0	1.7	dB
Voltage gain difference	$\|G_{V1} - G_{V2}\|$		0		2.0	dB

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. A protection diode is built-in between gate and source of transistor. However if forward current flows between gate and source transistor might be damaged. So please be careful not insert reverse.

3. *1: I_D is assured for I_{DSS}.

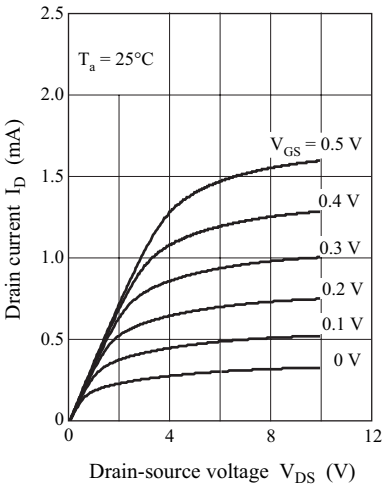
*2: Rank classification

Code	S	T
Rank	S	T
I_D (μA)	100 to 220	180 to 320
I_{DSS} (μA)	110 to 210	190 to 310
Marking Symbol	9S	9T

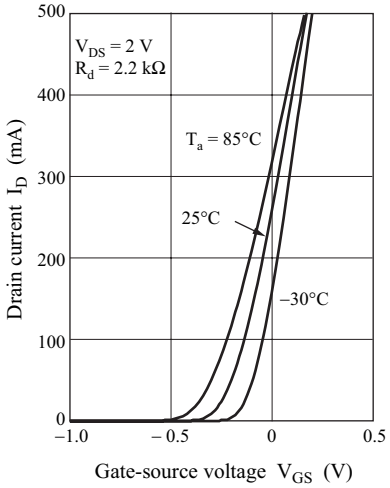
*3: NV is assured for design.

*4: $\Delta|G_V . f|$ is assured for AQL 0.065%. (The measurement method is used by source-grounded circuit.)

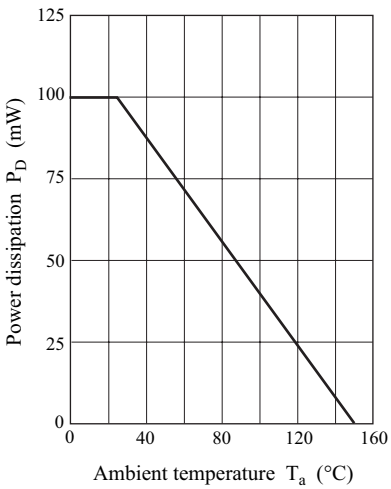
I_D — V_{DS}



I_D — V_{GS}

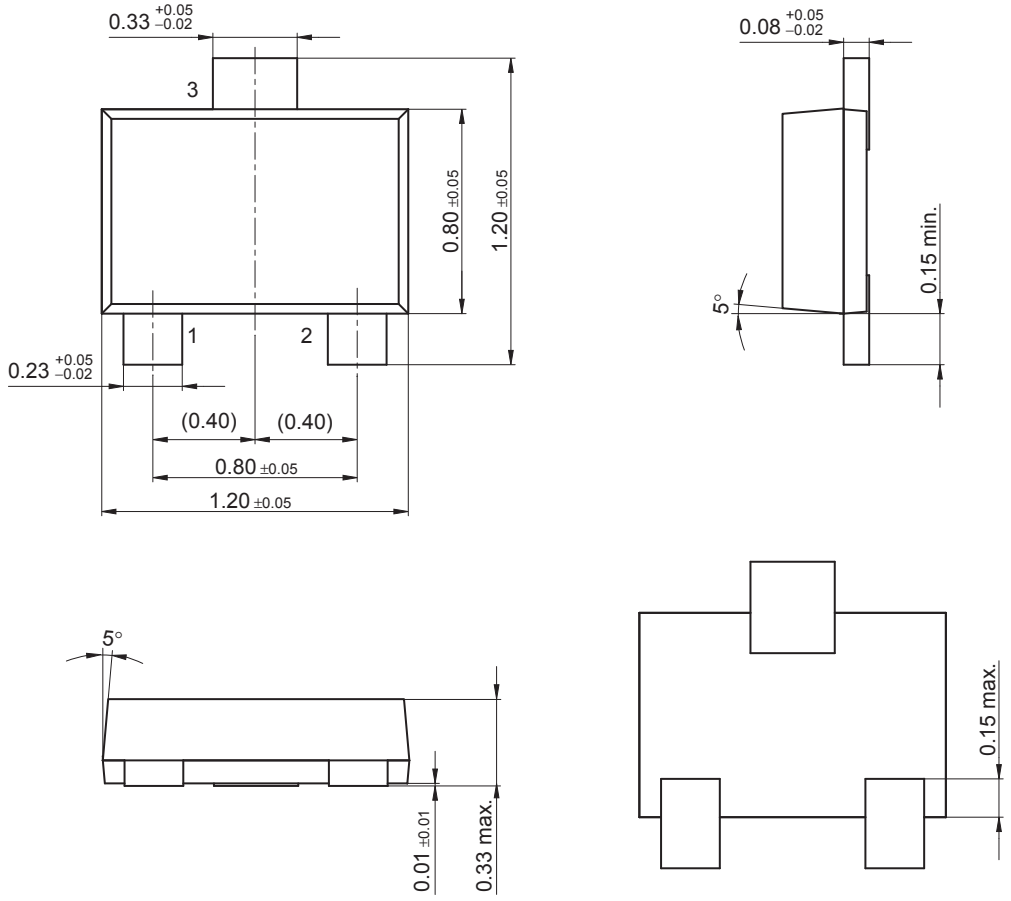


P_D — T_a



TSSSMini3-F2-B

Unit: mm



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