

DSK3J02

Silicon N-channel Junction FET

For impedance conversion in low frequency

■ Features

- Low noise voltage NV
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

■ Packaging

Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source voltage (Gate open)	V_{DSO}	20	V
Drain-gate voltage (Souece open)	V_{DGO}	20	V
Drain-source current (Gate open)	I_{DSO}	2	mA
Drain-gate current (Souece open)	I_{DGO}	2	mA
Power dissipation	P_{D}	100	mW
Operating ambient temperature	T_{opr}	-20 to +80	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

■ Package

- Code
SSSMini3-F2-B
- Pin Name
1: Drain
2: Source
3: Gate

■ Marking Symbol: 3

■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain current*1	I_{D}	$V_{\text{DS}} = 2.0 \text{ V}, R_{\text{d}} = 2.2 \text{ k}\Omega \pm 1\%$	100		470	μA
Drain-source cutoff current *2	I_{DSS}	$V_{\text{DS}} = 2.0 \text{ V}, R_{\text{d}} = 2.2 \text{ k}\Omega \pm 1\%, V_{\text{GS}} = 0$	110		460	μA
Forward transfer admittance	$ Y_{\text{fs}} $	$V_{\text{D}} = 2.0 \text{ V}, V_{\text{GS}} = 0, f = 1 \text{ MHz}$	660	1500		μS
Noise voltage *3	NV	$V_{\text{D}} = 2.0 \text{ V}, R_{\text{d}} = 2.2 \text{ k}\Omega \pm 1\%, C_{\text{O}} = 5 \text{ pF}, \text{A-curve}$			4	μV
Voltage gain	G_{V1}	$V_{\text{D}} = 2.0 \text{ V}, R_{\text{d}} = 2.2 \text{ k}\Omega \pm 1\%, C_{\text{O}} = 5 \text{ pF}, eG = 10 \text{ mV}, f = 1 \text{ kHz}$	-5.0	-1.0		dB
	G_{V2}	$V_{\text{D}} = 1.5 \text{ V}, R_{\text{d}} = 2.2 \text{ k}\Omega \pm 1\%, C_{\text{O}} = 5 \text{ pF}, eG = 10 \text{ mV}, f = 1 \text{ kHz}$	-7.0	-1.5		dB
	$\Delta G_{\text{V}} \cdot f $ *4	$V_{\text{D}} = 2.0 \text{ V}, R_{\text{d}} = 2.2 \text{ k}\Omega \pm 1\%, C_{\text{O}} = 5 \text{ pF}, eG = 10 \text{ mV}, f = 1 \text{ kHz to } 70 \text{ Hz}$		0	1.7	dB
Voltage gain difference	$ G_{\text{V1}} - G_{\text{V2}} $		0		2.0	dB

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. A protection diode is built-in between gate and source of transistor. However if forward current flows between gate and source transistor might be damaged. So please be careful not insert reverse.

3. *1: I_{D} is assured for I_{DSS} .

*2: Rank classification

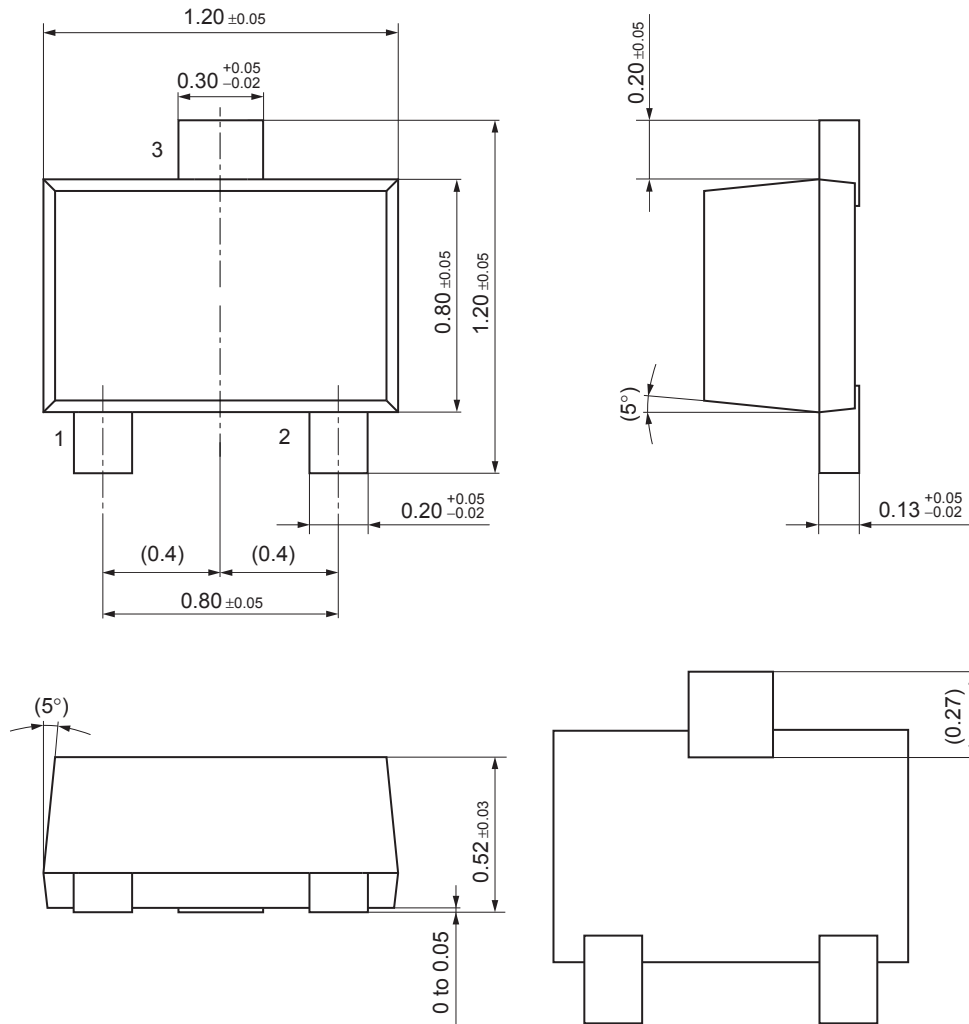
Code	S	T	U
Rank	S	T	U
I_{D} (μA)	100 to 220	180 to 320	280 to 470
I_{DSS} (μA)	110 to 210	190 to 310	290 to 460
Marking Symbol	3S	3T	3U

*3: NV is assured for design.

*4: $\Delta |G_{\text{V}} \cdot f|$ is assured for AQL 0.065%. (The measurement method is used by source-grounded circuit.)

SSSMini3-F2-B

Unit: mm



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