## MTMC8E2A

## Silicon N-channel MOS FET

For lithium-ion secondary battery protection circuit

#### Overview

The MTMC8E2A is the low ON resistance dual N-channel MOS FET designed for lithium-ion secondary battery protection circuit.

#### ■ Features

- $\bullet$  Low drain-source ON resistance:  $R_{DS(on)}$  typ. = 15 m  $\Omega$  (V  $_{GS}$  = 4.5 V)
- Small size surface mounting package: WMini8-F1 (2.9 mm × 2.8 mm × 0.8 mm)
- Drain common 2 elements
- Built-in gate resistor
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

#### Packaging

MTMC8E2A0L Embossed type (Thermo-compression sealing): 3000 pcs / reel (standard)

## ■ Absolute Maximum Ratings $T_a = 25$ °C

Parameter	Symbol	Rating	Unit	
Drain-source surrender voltage	V <sub>DSS</sub>	20	V	
Gate-source surrender voltage	V <sub>GSS</sub>	±12	V	
Drain current	$I_D$	7.0	A	
Peak drain current	$I_{DP}$	42	A	
Power dissipation	P <sub>D</sub> 1*1	1.0	W	
	P <sub>D</sub> 2 *1, *2	1.2		
	P <sub>D</sub> 3*3	0.4		
Channel temperature	T <sub>ch</sub>	150	°C	
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

Note) \*1: Glass epoxy board:  $25.4 \text{ mm} \times 25.4 \text{ mm} \times 0.8 \text{ mm}$ 

Copper foil of the drain portion should have a area of  $300\ mm^2$  or more

- \*2: t = 10 s
- \*3: Stand-alone (without the board)

#### ■ Package

• Code

WMini8-F1

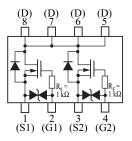
Package dimension clicks here.  $\rightarrow$ 

#### • Pin Name

1: Source-1	5: Drain
2: Gate-1	6: Drain
3: Source-2	7: Drain
4: Gate-2	8: Drain

### ■ Marking Symbol: 4B

#### ■ Internal Connection



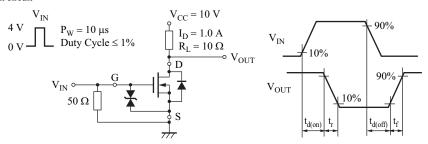
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## ■ Electrical Characteristics $T_a = 25$ °C±3°C

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source surrender voltage	V <sub>DSS</sub>	$I_D = 1.0 \text{ mA}, V_{GS} = 0$	20			V
Drain-source cutoff current	$I_{DSS}$	$V_{DS} = 20 \text{ V}, V_{GS} = 0$			1.0	μА
Gate-source cutoff current	$I_{GSS}$	$V_{GS} = \pm 8.0 \text{ V}, V_{DS} = 0$			±10	μΑ
Gate threshold voltage	V <sub>TH</sub>	$I_D = 1.0 \text{ mA}, V_{DS} = 10 \text{ V}$	0.40	0.85	1.30	V
Drain-source ON resistance 1	R <sub>DS(on)</sub> 1	$I_D = 2.0 \text{ A}, V_{GS} = 4.5 \text{ V}$		15	21	mΩ
Drain-source ON resistance 2	R <sub>DS(on)</sub> 2	$I_D = 2.0 \text{ A}, V_{GS} = 3.7 \text{ V}$		18	25	mΩ
Drain-source ON resistance 3	R <sub>DS(on)</sub> 3	$I_D = 1.0 \text{ A}, V_{GS} = 2.5 \text{ V}$		22	33	mΩ
Forward transfer admittance	Y <sub>fs</sub>	$I_D = 1.0 \text{ A}, V_{DS} = 10 \text{ V}$	3.0			S
Short-circuit input capacitance (Common source)	C <sub>iss</sub>			1450		pF
Short-circuit output capacitance (Common source)	C <sub>oss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		100		pF
Reverse transfer capacitance (Common source)	C <sub>rss</sub>			90		pF
Turn-on delay time *	t <sub>d(on)</sub>	$V_{DD} = 10 \text{ V}, V_{GS} = 0 \text{ V to 4 V},$ $I_D = 1.0 \text{ A}$		0.33		μs
Rise time *	t <sub>r</sub>			0.70		μs
Turn-off delay time *	t <sub>d(off)</sub>	$V_{DD} = 10 \text{ V}, V_{GS} = 4 \text{ V to } 0 \text{ V},$		4.0		μs
Fall time *	$t_{\rm f}$	$I_D = 1.0 \text{ A}$		2.0		μs

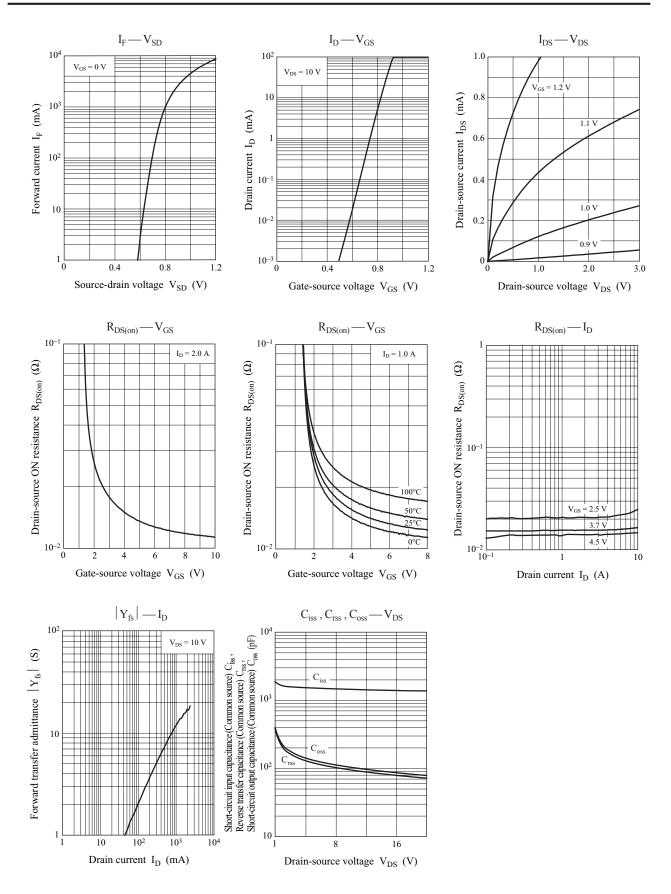
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

#### 2. \*: Measurement circuit



2 Ver. EED

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