

MTM98240

Silicon N-channel MOS FET

For DC-DC converter circuits

For LCD back light inverter

■ Overview

The MTM98240 is suitable for DC-DC converter and LCD back light inverter, which features the industry's top-class low on-resistance and switching characteristics with fine process.

■ Features

- Low on-resistance: $R_{on} = 16 \text{ m}\Omega$ typ. ($V_{GS} = 10 \text{ V}$)
- High speed switching characteristic
- Halogen free
- Flat-lead package: SO8-F1-B

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	40	V
Gate-source surrender voltage	V_{GSS}	± 20	V
Drain current	I_D	7	A
Peak drain current	I_{DP}	28	A
Power dissipation *	P_D	2	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Note) *: Measuring on ceramic substrate at 50 mm × 50 mm × 1.0 mm

■ Package

• Code

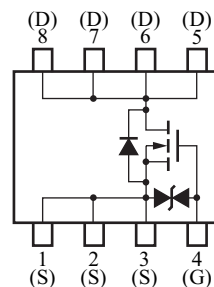
SO8-F1-B

• Pin Name

1: Source	5: Drain
2: Source	6: Drain
3: Source	7: Drain
4: Gate	8: Drain

■ Marking Symbol: CA

■ Internal Connection

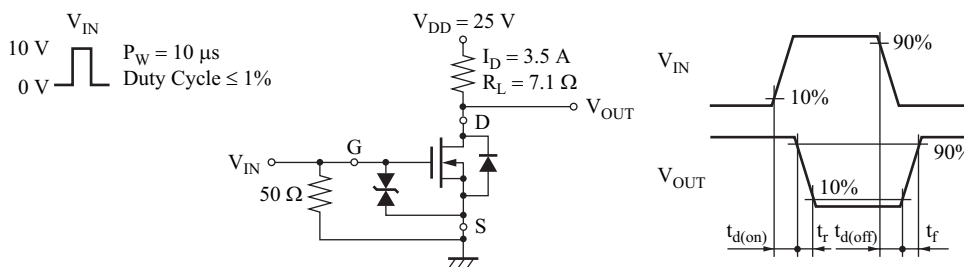


■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	$I_D = 1 \text{ mA}, V_{GS} = 0$	40			V
Drain-source cutoff current	I_{DSS}	$V_{DS} = 40 \text{ V}, V_{GS} = 0$			10	μA
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$			± 10	μA
Gate threshold voltage	V_{TH}	$I_D = 1.0 \text{ mA}, V_{DS} = 10.0 \text{ V}$	1.0		2.5	V
Drain-source ON resistance *1	$R_{DS(on)}$	$I_D = 7 \text{ A}, V_{GS} = 10 \text{ V}$		16	23	m Ω
		$I_D = 3.5 \text{ A}, V_{GS} = 5.0 \text{ V}$		29	40	
Forward transfer conductance	$ Y_{fs} $	$I_D = 7 \text{ A}, V_{DS} = 10 \text{ V}$	4			S
Short-circuit input capacitance (Common source)	C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		1 750		pF
Short-circuit output capacitance (Common source)	C_{oss}			150		pF
Reverse transfer capacitance (Common source)	C_{rss}			90		pF
Turn-on delay time *1, *2	$t_{d(on)}$	$V_{DD} = -25 \text{ V}, V_{GS} = 0 \text{ V to } -10 \text{ V},$ $I_D = 3.5 \text{ A}$		17		ns
Rise time *1, *2	t_r			9		ns
Turn-off delay time *1, *2	$t_{d(off)}$	$V_{DD} = -25 \text{ V}, V_{GS} = -10 \text{ V to } 0 \text{ V},$ $I_D = 3.5 \text{ A}$		94		ns
Fall time *1, *2	t_f			33		ns

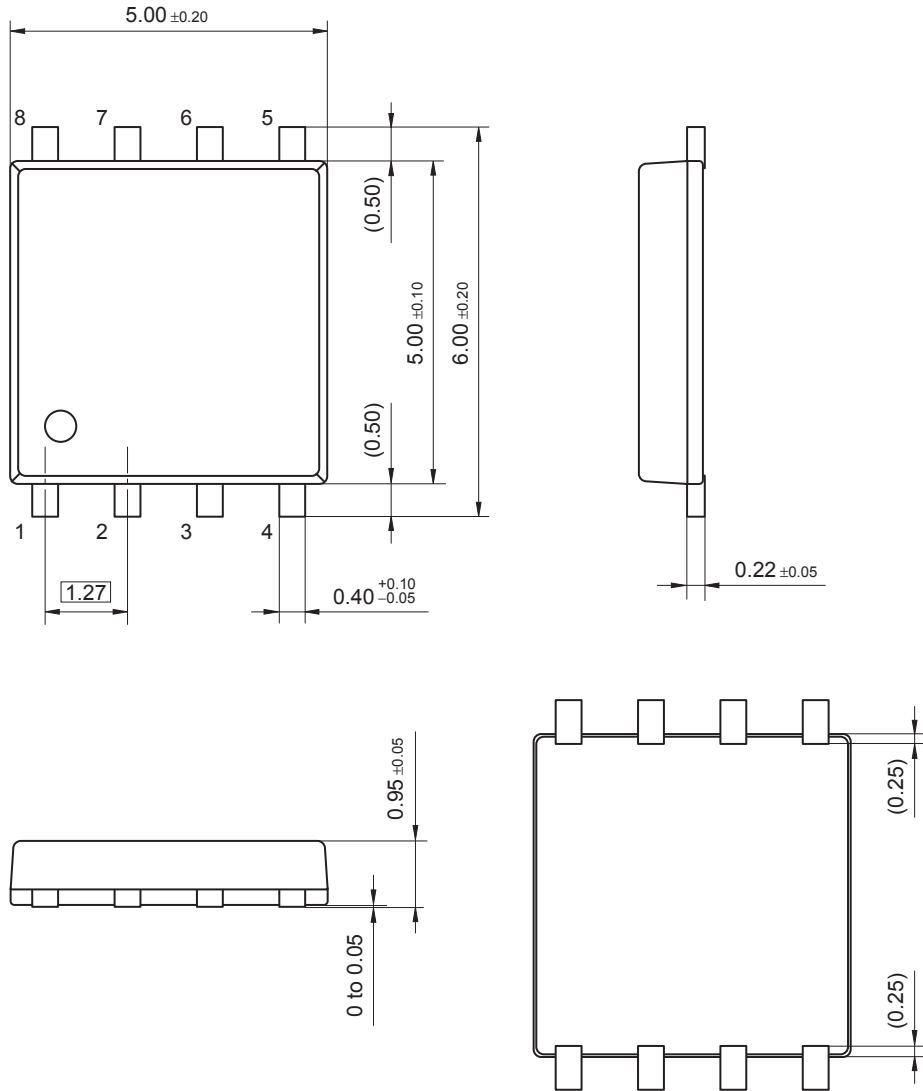
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

- 2. *1: Pulse measurement
- *2: Measurement circuit



SO8-F1-B

Unit: mm



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