MTM86127

Silicon P-channel MOS FET

For DC-DC converter circuits

■ Overview

MTM86127 is the low on resistance P-channel MOS FET designed for DC-DC converter circuits.

■ Features

- Low drain-source ON resistance: $R_{DS(on)}$ typ. = 140 mΩ (V_{GS} = –1.8 V)
- Low drive voltage: 1.8 V drive
- Small package: WSSMini6-F1
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

■ Packaging

Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

■ Absolute Maximum Ratings T_a = 25°C

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	–20	V
Gate-source surrender voltage	V_{GSS}	±10	V
Drain current	I_D	–2.0	A
Peak drain current	I_{DP}	–8.0	A
Power dissipation *	P_D	540	mW
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

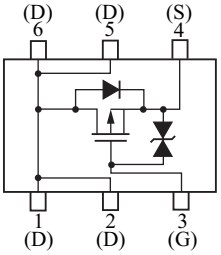
Note) *: Measuring on ceramic substrate at 40 mm × 38 mm × 0.2 mm
P_D absolute maximum rating without a heat shink: 150 mW

■ Package

- Code
  WSSMini6-F1
- Pin Name
  1: Drain 4: Source
  2: Drain 5: Drain
  3: Gate 6: Drain

■ Marking Symbol: MK

■ Internal Connection



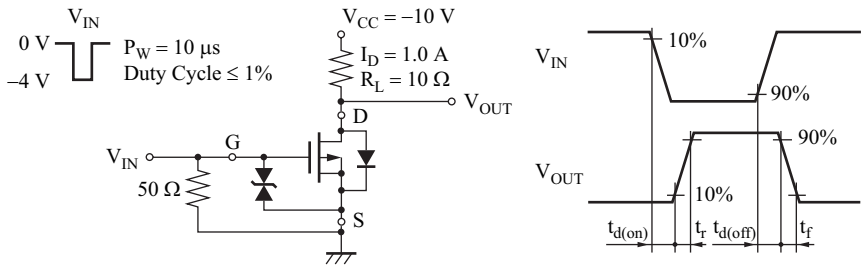
■ Electrical Characteristics $T_a = 25°C \pm 3°C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	$I_D = -1.0$ mA, $V_{GS} = 0$	–20			V
Drain-source cutoff current	I_{DSS}	$V_{DS} = -20$ V, $V_{GS} = 0$			–1.0	μA
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 8$ V, $V_{DS} = 0$			±10	μA
Gate threshold voltage	V_{TH}	$I_D = -1.0$ mA, $V_{DS} = -10$ V	– 0.40	– 0.75	–1.10	V
Drain-source ON resistance 1 *1	$R_{DS(on)}1$	$I_D = -1.0$ A, $V_{GS} = -4.0$ V		80	120	mΩ
Drain-source ON resistance 2 *1	$R_{DS(on)}2$	$I_D = -1.0$ A, $V_{GS} = -2.5$ V		100	170	mΩ
Drain-source ON resistance 3 *1	$R_{DS(on)}3$	$I_D = -0.5$ A, $V_{GS} = -1.8$ V		140	230	mΩ
Forward transfer admittance *1	$\lvert Y_{fs} \rvert$	$I_D = -1.0$ A, $V_{DS} = -10$ V, f = 1 kHz	3.0			S
Short-circuit input capacitance (Common source)	C_{iss}	$V_{DS} = -10$ V, $V_{GS} = 0$, f = 1 MHz		300		pF
Short-circuit output capacitance (Common source)	C_{oss}			30		pF
Reverse transfer capacitance (Common source)	C_{rss}			35		pF
Turn-on delay time *2	$t_{d(on)}$	$V_{DD} = -10$ V, $V_{GS} = 0$ V to –4 V, $I_D = -1.0$ A		6		ns
Rise time *2	t_r			8		ns
Turn-off delay time *2	$t_{d(off)}$	$V_{DD} = -10$ V, $V_{GS} = -4$ V to 0 V, $I_D = -1.0$ A		57		ns
Fall time *2	t_f			55		ns

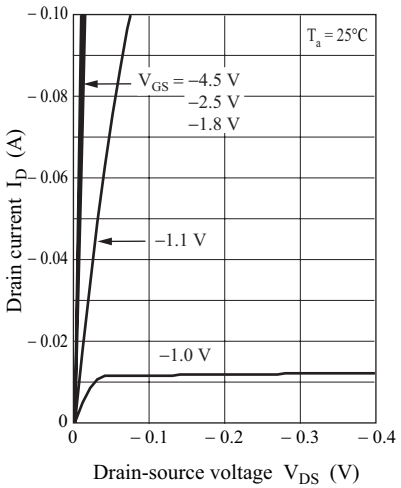
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *1: Pulse measurement

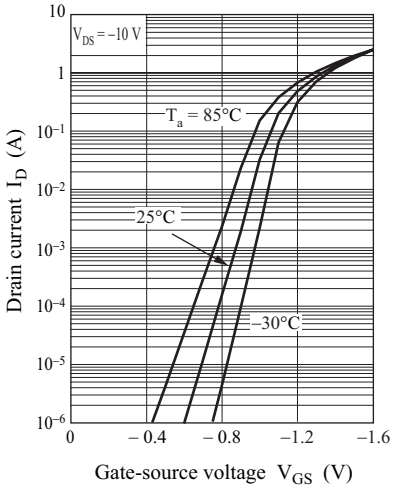
*2: Test circuit



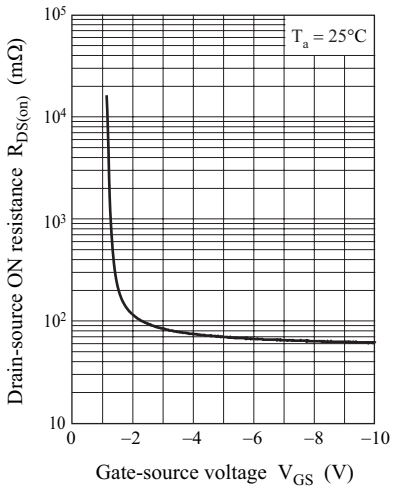
I_D — V_{DS}



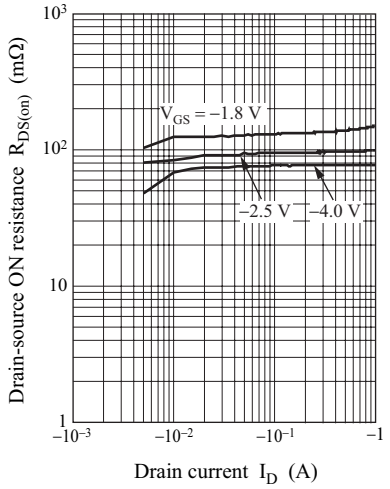
I_D — V_{GS}



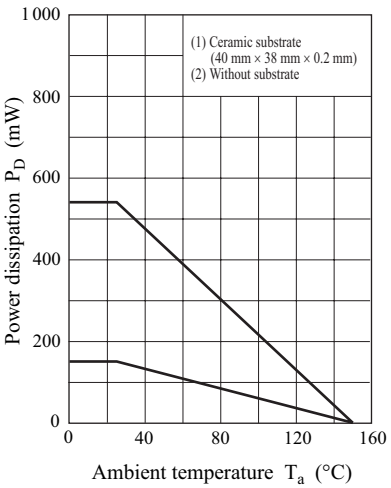
$R_{DS(on)}$ — V_{GS}



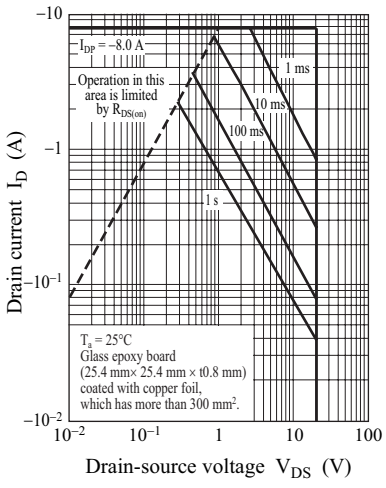
$R_{DS(on)}$ — I_D



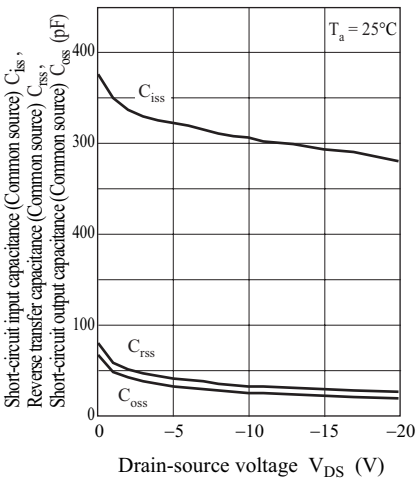
P_D — T_a



Safe operation area



C_{iss} , C_{oss} , C_{rss} — V_{DS}



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