MTM76320

Silicon N-channel MOS FET (FET1)
Silicon P-channel MOS FET (FET2)

For DC-DC converter circuits
For switching circuits

■ Overview

MTM76320 is the composite MOS FET (N-channel and P-channel MOS FET) that is highly suitable for DC-DC converter and other switching circuits.

■ Features

- N-channel + P-channel MOS FET in one package
- Low drain-source ON resistance: $R_{DS(on)}$ typ. =
  N-ch. : 80 mΩ (V_{GS} = 4.0 V), P-ch. : 100 mΩ (V_{GS} = –4.0 V)
- Small size surface mounting package: WSMini6-F1-B (2.1 mm × 2.0 mm × 0.7 mm)
- 2.5 V drive
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

■ Packaging

MTM763200L Embossed type (Thermo-compression sealing): 3000 pcs / reel (standard)

■ Absolute Maximum Ratings T_a = 25°C

Parameter		Symbol	Rating	Unit
FET1 (N-ch.)	Drain-source surrender voltage	V_{DSS}	20	V
	Gate-source surrender voltage	V_{GSS}	±10	V
	Drain current	I_D	1.9	A
	Peak drain current	I_{DP}	12	A
FET2 (P-ch.)	Drain-source surrender voltage	V_{DSS}	–20	V
	Gate-source surrender voltage	V_{GSS}	±10	V
	Drain current	I_D	–1.2	A
	Peak drain current	I_{DP}	–7	A
Overall	Total power dissipation *	P_D	700	mW
	Channel temperature	T_{ch}	150	°C
	Storage temperature	T_{stg}	–55 to +150	°C

Note) *: Measuring on ceramic substrate at 40 mm × 38 mm × 0.2 mm
P_D absolute maximum rating without a heat shink: 150 mW

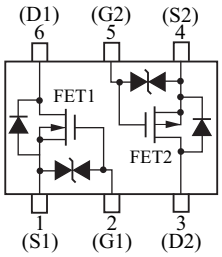
■ Package

- Code
  WSMini6-F1-B
  Package dimension clicks here.→ Click!

- Pin Name
  1. Source (FET1)
  2. Gate (FET1)
  3. Drain (FET2)
  4. Source (FET2)
  5. Gate (FET2)
  6. Drain (FET1)

■ Marking Symbol: JB

■ Internal Connection



■ Electrical Characteristics $T_a = 25°C \pm 3°C$

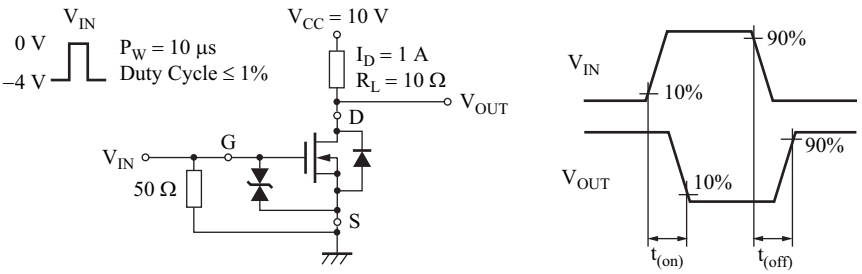
• FET1 (N-ch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	$I_D = 1$ mA, $V_{GS} = 0$ V	20			V
Drain-source cutoff current	I_{DSS}	$V_{DS} = 20$ V, $V_{GS} = 0$ V			1.0	μA
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 8.0$ V, $V_{DS} = 0$ V			±10	μA
Gate threshold voltage	V_{TH}	$I_D = 1.0$ mA, $V_{DS} = 10$ V	0.4	0.85	1.3	V
Drain-source ON resistance 1 *1	$R_{DS(on)}1$	$I_D = 1$ A, $V_{GS} = 4.0$ V		80	105	mΩ
Drain-source ON resistance 2 *1	$R_{DS(on)}2$	$I_D = 0.5$ A, $V_{GS} = 2.5$ V		100	150	mΩ
Forward transfer admittance *1	$\lvert Y_{fs} \rvert$	$I_D = 1.0$ A, $V_{DS} = 10$ V	3.0			S
Short-circuit input capacitance (Common source)	C_{iss}	$V_{DS} = 10$ V, $V_{GS} = 0$ V, f = 1 MHz		280		pF
Short-circuit output capacitance (Common source)	C_{oss}			18		pF
Reverse transfer capacitance (Common source)	C_{rss}			17		pF
Turn-on time *2	t_{on}	$V_{DD} = 10$ V, $V_{GS} = 0$ V to 4 V, $I_D = 1$ A		12		ns
Turn-off time *2	t_{off}	$V_{DD} = 10$ V, $V_{GS} = 4$ V to 0 V, $I_D = 1$ A		50		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *1: Pulse measurement

*2: Test circuit



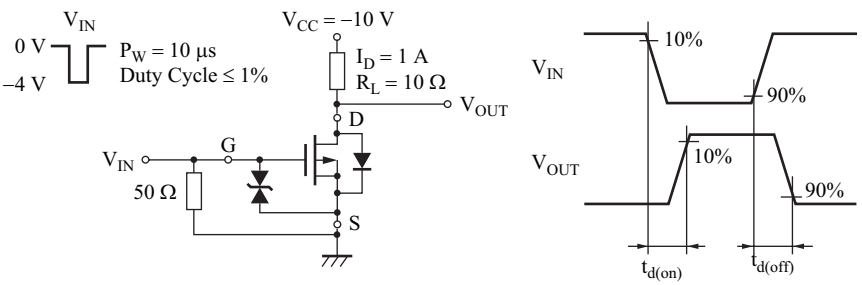
• FET2 (P-ch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	$I_D = -1$ mA, $V_{GS} = 0$ V	–20			V
Drain-source cutoff current	I_{DSS}	$V_{DS} = -20$ V, $V_{GS} = 0$ V			–1.0	μA
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 8.0$ V, $V_{DS} = 0$ V			±10	μA
Gate threshold voltage	V_{TH}	$I_D = -1.0$ mA, $V_{DS} = -10$ V	– 0.4	– 0.85	–1.3	V
Drain-source ON resistance 1 *1	$R_{DS(on)}1$	$I_D = -1$ A, $V_{GS} = -4.0$ V		100	130	mΩ
Drain-source ON resistance 2 *1	$R_{DS(on)}2$	$I_D = -0.6$ A, $V_{GS} = -2.5$ V		130	200	mΩ
Forward transfer admittance *1	$\lvert Y_{fs} \rvert$	$I_D = -1.0$ A, $V_{DS} = -10$ V	3.0			S
Short-circuit input capacitance (Common source)	C_{iss}	$V_{DS} = -10$ V, $V_{GS} = 0$ V, f = 1 MHz		440		pF
Short-circuit output capacitance (Common source)	C_{oss}			40		pF
Reverse transfer capacitance (Common source)	C_{rss}			38		pF
Turn-on time *2	t_{on}	$V_{DD} = -10$ V, $V_{GS} = 0$ V to –4 V, $I_D = -1$ A		35		ns
Turn-off time *2	t_{off}	$V_{DD} = -10$ V, $V_{GS} = -4$ V to 0 V, $I_D = -1$ A		100		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

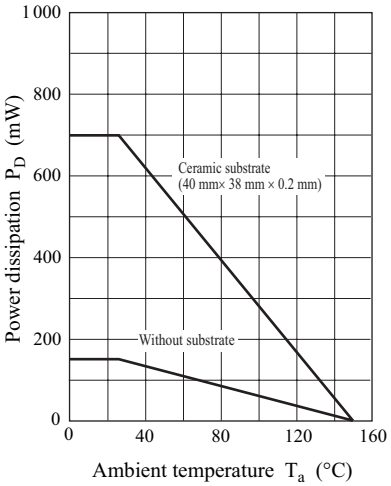
2. *1: Pulse measurement

*2: Test circuit



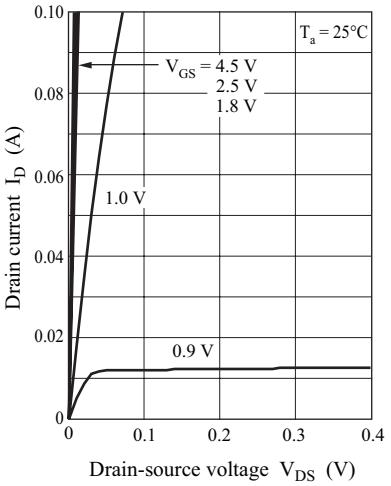
Common characteristics chart

P_D — T_a

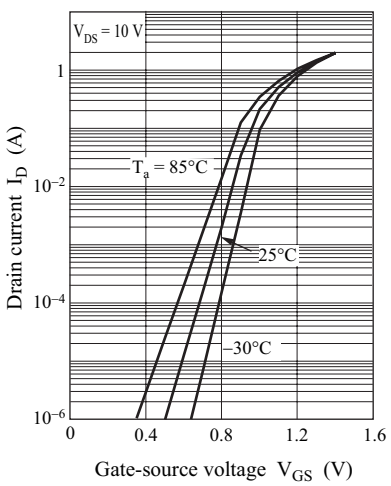


Characteristics charts of FET1

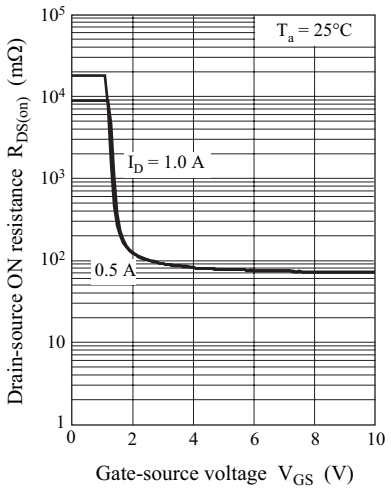
I_D — V_{DS}



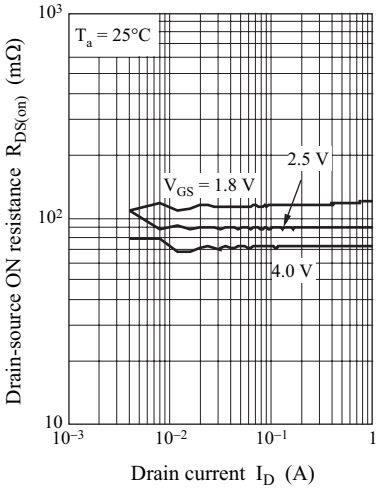
I_D — V_{GS}



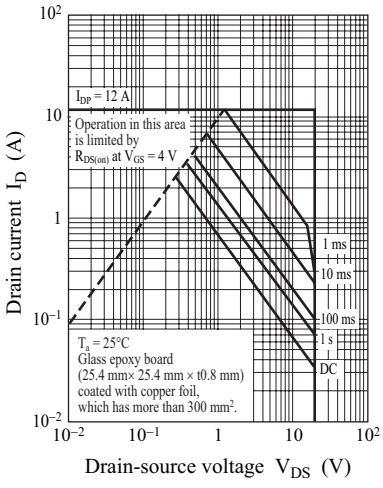
$R_{DS(on)}$ — V_{GS}



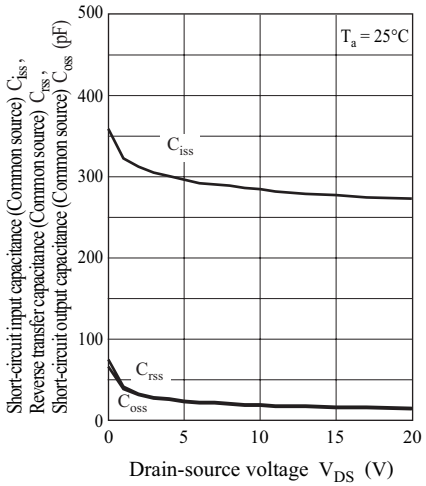
$R_{DS(on)}$ — I_D



Safe operation area

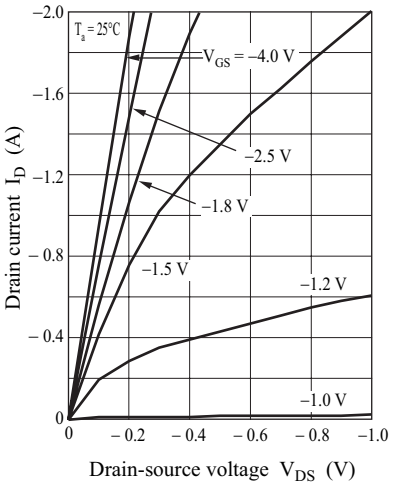


C_{iss} , C_{rss} , C_{oss} — V_{DS}

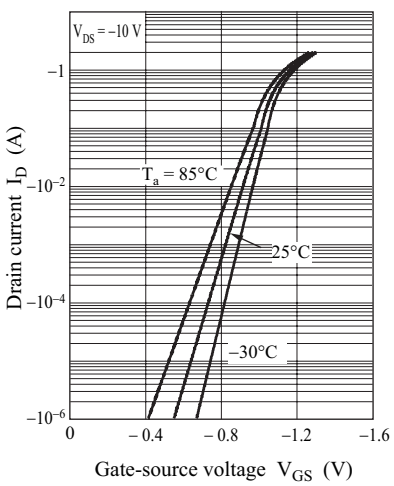


Characteristics charts of FET2

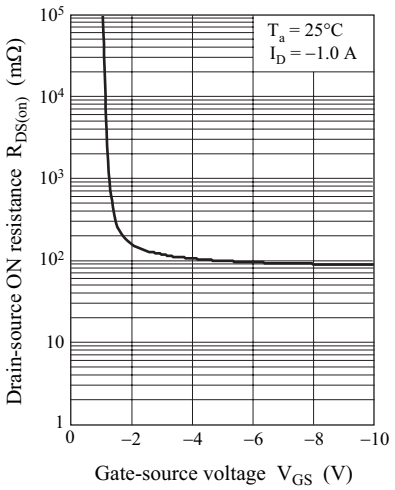
I_D — V_{DS}



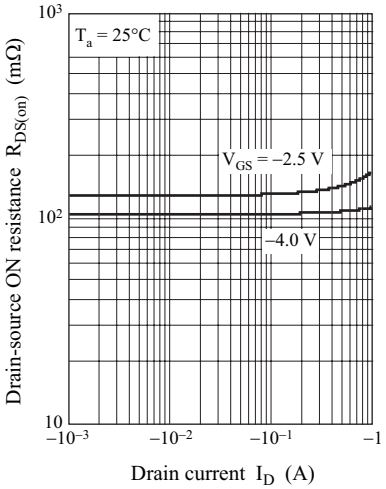
I_D — V_{GS}



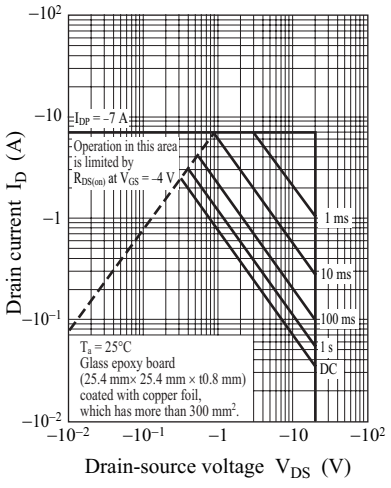
$R_{DS(on)}$ — V_{GS}



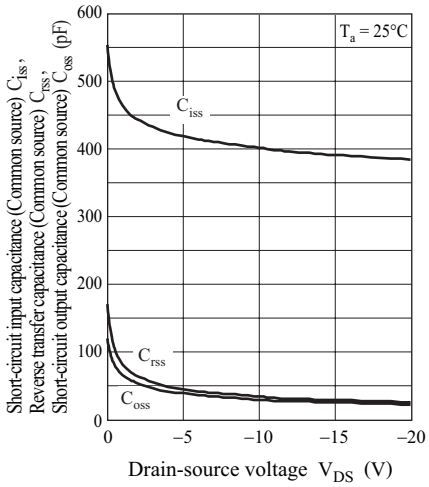
$R_{DS(on)}$ — I_D



Safe operation area



C_{iss} , C_{rss} , C_{oss} — V_{DS}



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