MTM68410

Silicon P-channel MOS FET

For load switch circuits
For switching circuits

■ Overview

MTM68410 is the low ON resistance dual P-channel MOS FET designed for load switch circuits.

■ Features

- Dual P-channel MOS FET in one package
- Low ON resistance: R_{on} = 32 mΩ (V_{GS} = –4.0 V)
- Small package and surface mounting type: WMini8-F1 (2.8 mm × 2.9 mm × 1.0 mm)
- Low drive voltage: 1.8 V drive

■ Packaging

MTM684100L Embossed type (Thermo-compression sealing): 3000 pcs / reel (standard)

■ Absolute Maximum Ratings T_a = 25°C

Parameter	Symbol	Rating	Unit
Drain-source surrender voltage	V_{DSS}	–12	V
Gate-source surrender voltage	V_{GSS}	±8	V
Drain current	I_D	–4.8	A
Peak drain current	I_{DP}	–19	A
Power dissipation *	P_D	1.0	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

Note) *: Glass epoxy board: 25.4 mm × 25.4 mm × 0.8 mm
Copper foil of the drain portion should have a area of 300 mm² or more
P_D absolute maximum rating without a heat shink: 400 mW

■ Package

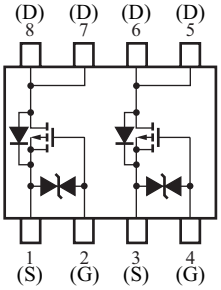
- Code
  WMini8-F1
  Package dimension clicks here.→ Click!

- Pin Name

1: Source	5: Drain
2: Gate	6: Drain
3: Source	7: Drain
4: Gate	8: Drain

■ Marking Symbol: 1C

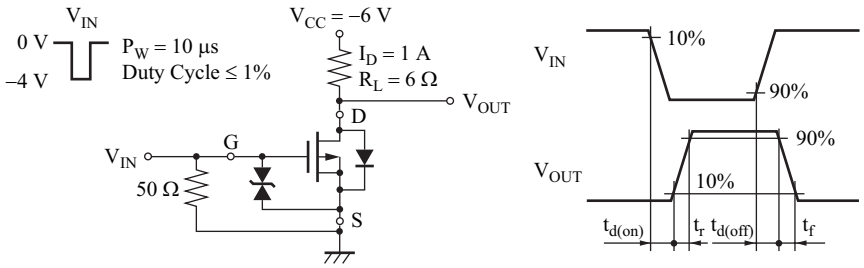
■ Internal Connection



■ Electrical Characteristics T_a = 25°C±3°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = –1 mA, V_{GS} = 0	–12			V
Drain-source cutoff current	I_{DSS}	V_{DS} = –12 V, V_{GS} = 0			–1.0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±6.4 V, V_{DS} = 0			±10	μA
Gate threshold voltage	V_{TH}	I_D = –1.0 mA, V_{DS} = –6.0 V	– 0.3	– 0.65	–1.0	V
Drain-source ON resistance	$R_{DS(on)}1$	I_D = –1 A, V_{GS} = –4.0 V		32	42	mΩ
	$R_{DS(on)}2$	I_D = – 0.5 A, V_{GS} = –2.5 V		37	55	
	$R_{DS(on)}3$	I_D = – 0.2 A, V_{GS} = –1.8 V		50	75	
Forward transfer admittance	$\|Y_{fs}\|$	I_D = –1.0 A, V_{DS} = –10 V	3.5			S
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz		1 200		pF
Short-circuit output capacitance (Common source)	C_{oss}			110		pF
Reverse transfer capacitance (Common source)	C_{rss}			110		pF
Turn-on delay time *	$t_{d(on)}$	V_{DD} = –6 V, V_{GS} = 0 V to –4 V, I_D = –1 A		8		ns
Rise time *	t_r			11		ns
Turn-off delay time *	$t_{d(off)}$	V_{DD} = –6 V, V_{GS} = –4 V to 0 V, I_D = –1 A		235		ns
Fall time *	t_f			85		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *: Test circuit



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