FL6L5203

Silicon P-channel MOS FET (FET)
Silicon epitaxial planar type (SBD)

For DC-DC converter circuits
For switching circuits

■ Overview

FL6L5203 is P-channel type MOS FET with Schottky Brrier Diode in small size surface mouting pakcage.

■ Features

- Low drive voltage: 2.5 V
- Low forward voltage V_F
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

■ Packaging

FL6L52030L Embossed type (Thermo-compression sealing): 10000 pcs / reel (standard)

■ Absolute Maximum Ratings $T_a = 25°C$

Parameter		Symbol	Rating	Unit
FET	Drain-source surrender voltage	V_{DSS}	–20	V
	Gate-source surrender voltage	V_{GSS}	±12	V
	Drain current	I_D	–1.0	A
	Peak drain current	I_{DP}	–4.0	A
	Channel temperature	T_{ch}	150	°C
SBD	Reverse voltage	V_R	20	V
	Forward current (Average)	$I_{F(AV)}$	800	mA
	Junction temperature	T_j	125	°C
Overall	Total power dissipation *	P_D	540	mW
	Storage temperature	T_{stg}	–55 to +125	°C

Note) *: Measuring on ceramic substrate at (40 mm × 38 mm × 0.2 mm)
Absolute maximum rating without heat sink for P_D is 150 mW

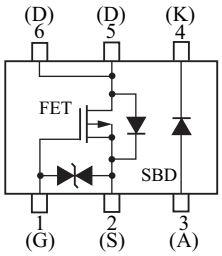
■ Package

- Code
  WSSMini6-F1
  Package dimension clicks here.→ Click!

- Pin Name
  1: Gate 4: Cathode
  2: Source 5: Drain
  3: Anode 6: Drain

■ Marking Symbol: Y3

■ Internal Connection

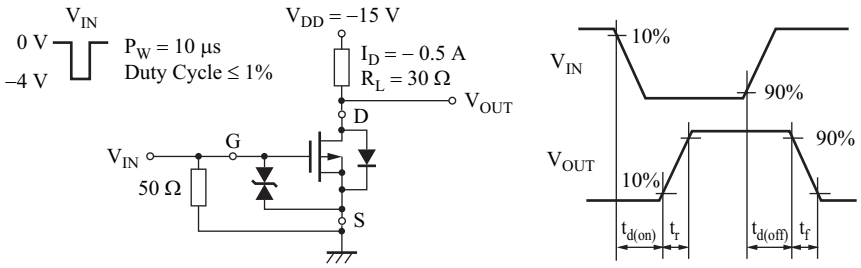


■ Electrical Characteristics T_a = 25°C±3°C

• FET

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = –1.0 mA, V_{GS} = 0	–20			V
Drain-source cutoff current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0			–1.0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0			±10	μA
Gate threshold voltage	V_{TH}	I_D = –1.0 μA, V_{DS} = –10 V	– 0.45	–1.0	–1.5	V
Drain-source ON resistance *1	$R_{DS(on)}$	I_D = – 0.5 mA, V_{GS} = –4.0 V		300	420	mΩ
		I_D = – 0.5 mA, V_{GS} = –2.5 V		420	560	
Forward transfer admittance *1	$\|Y_{fs}\|$	I_D = – 0.5 mA, V_{DS} = –10 V, f = 1 MHz	1.0			S
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz		80		pF
Short-circuit output capacitance (Common source)	C_{oss}			12		pF
Reverse transfer capacitance (Common source)	C_{rss}			12		pF
Turn-on delay time *2	$t_{d(on)}$	V_{DD} = –15 V, V_{GS} = 0 V to –4 V, I_D = –1.0 A		12		ns
Rise time *2	t_r			6		ns
Turn-off delay time *2	$t_{d(off)}$	V_{DD} = –15 V, V_{GS} = –4 V to 0 V, I_D = –1.0 A		17		ns
Fall time *2	t_f			10		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *1: Pulse measurement
*2: Test circuit



• SBD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Forward voltage	V_F	I_F = 800 mA			0.47	V
Reverse current	I_R	V_R = 20 V			80	μA

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7031 measuring methods for diodes.

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