FL525205

Silicon P-channel MOS FET (FET)
Silicon epitaxial planar type (SBD)

For DC-DC converter circuits
For switching circuits

■ Overview

FL525205 is the P-channel single type small signal MOS FET with SBD.

■ Features

- Low drain-source ON resistance: $R_{DS(on)}$ typ. = 100 mΩ (V_{GS} = –4.0 V)
- Composide with schottky barrier diode
- Small size surface mounting package: Mini5-G3-B (2.8 mm × 2.9 mm × 1.1 mm)
- Contributes to miniaturization of sets, mount area reduction
- Eco-friendly Halogen-free package

■ Packaging

FL5252050L Embossed type (Thermo-compression sealing): 3000 pcs / reel (standard)

■ Absolute Maximum Ratings T_a = 25°C

Parameter		Symbol	Rating	Unit
FET	Drain-source surrender voltage	V_{DSS}	–20	V
	Gate-source surrender voltage	V_{GSS}	±10	V
	Drain current	I_D	–2.1	A
	Peak drain current	I_{DP}	–8	A
	Channel temperature	T_{ch}	125	°C
SBD	Reverse voltage	V_R	20	V
	Forward current (Average)	$I_{F(AV)}$	700	mA
	Junction temperature	T_j	125	°C
Overall	Total power dissipation *	P_D	600	mW
	Storage temperature	T_{stg}	–55 to +125	°C

Note) *: Measuring on ceramic substrate at (40 mm × 38 mm × 0.2 mm)
Absolute maximum rating without heat sink for P_D is 300 mW

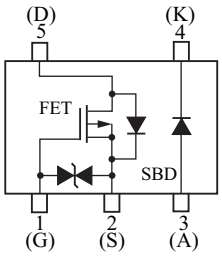
■ Package

- Code
  Mini5-G3-B
  Package dimension clicks here.→ Click!

- Pin Name
  1: Gate
  2: Source
  3: Anode
  4: Cathode
  5: Drain

■ Marking Symbol: Y0

■ Internal Connection

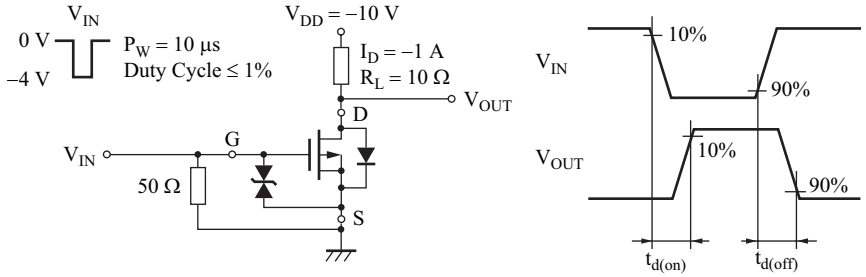


■ Electrical Characteristics T_a = 25°C±3°C

• FET

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = –1 mA, V_{GS} = 0 V	–20			V
Drain-source cutoff current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0 V			–1.0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA
Gate threshold voltage	V_{TH}	I_D = –1.0 mA, V_{DS} = –10 V	– 0.4	– 0.85	–1.3	V
Drain-source ON resistance *1	$R_{DS(on)}$	I_D = –1.0 A, V_{GS} = –4.0 V		100	130	mΩ
		I_D = – 0.5 A, V_{GS} = –2.5 V		130	200	
Forward transfer admittance *1	$\|Y_{fs}\|$	I_D = –1.0 A, V_{DS} = –10 V	3.0			S
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} = –10 V, V_{GS} = 0 V, f = 1 MHz		400		pF
Short-circuit output capacitance (Common source)	C_{oss}			40		pF
Reverse transfer capacitance (Common source)	C_{rss}			35		pF
Turn-on delay time *2	$t_{d(on)}$	V_{DD} = –10 V, V_{GS} = 0 V to –4 V, I_D = –1.0 A		35		ns
Turn-off delay time *2	$t_{d(off)}$	V_{DD} = –10 V, V_{GS} = –4 V to 0 V, I_D = –1.0 A		100		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. ∗1: Pulse measurement
∗2: Test circuit



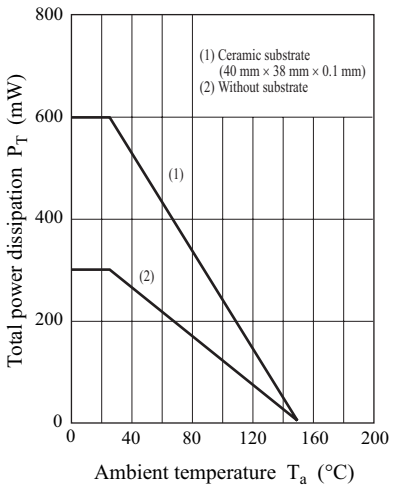
• SBD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Forward voltage	V_F	I_F = 700 mA			0.45	V
Reverse current	I_R	V_R = 20 V			200	μA
Terminal capacitance	C_t	V_R = 10 V, f = 1 MHz		12		pF
Reverse recovery time	t_{rr}	I_F = I_R = 100 mA, I_{rr} = 10 mA		4.3		ns

Note) Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7031 measuring methods for diodes.

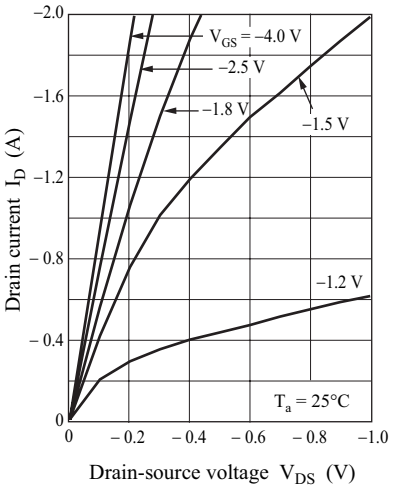
Common characteristics chart

P_T — T_a

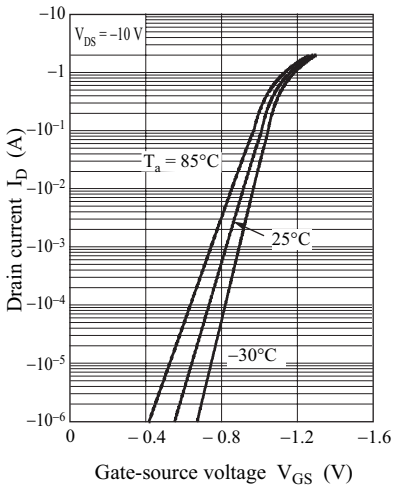


Characteristics charts of FET

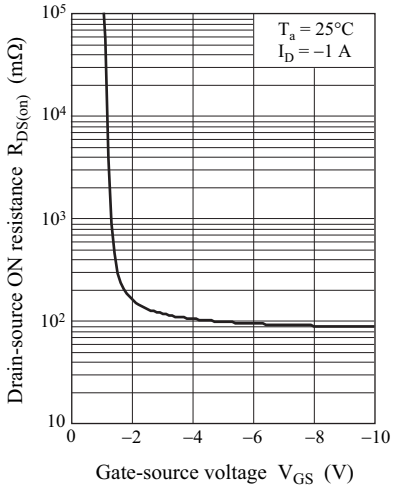
I_D — V_{DS}



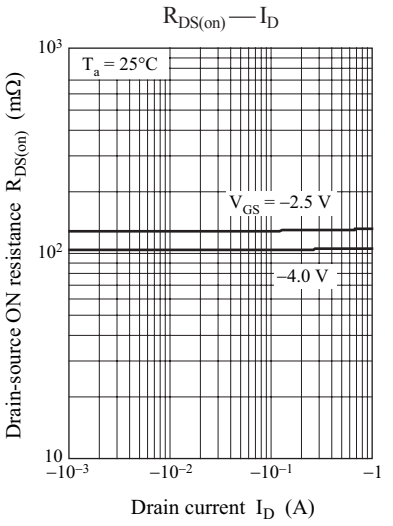
I_D — V_{GS}



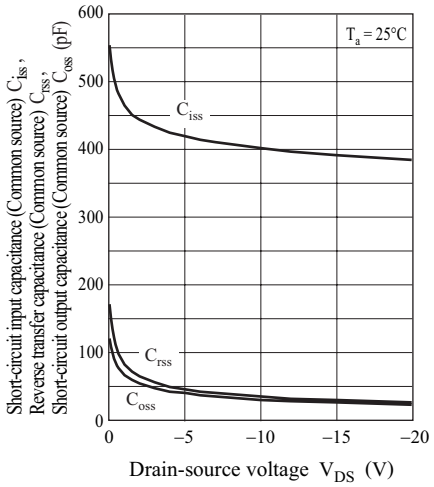
$R_{DS(on)}$ — V_{GS}



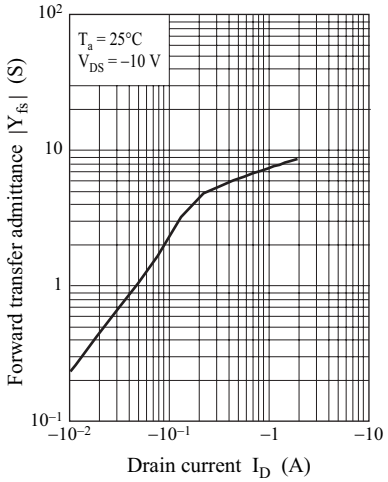
$R_{DS(on)}$ — I_D



C_{iss} , C_{rss} , C_{oss} — V_{DS}

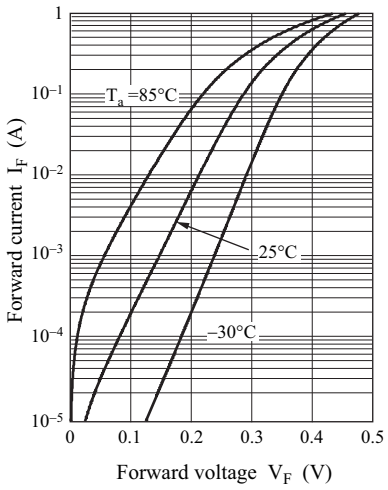


$|Y_{fs}|$ — I_D

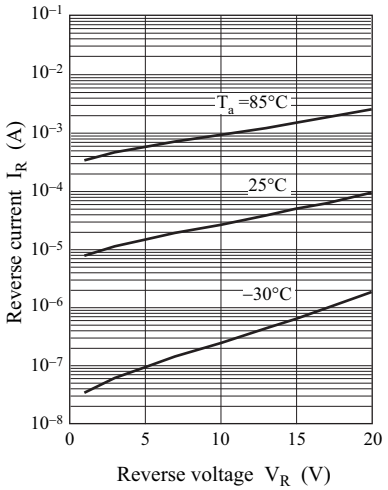


Characteristics charts of SBD

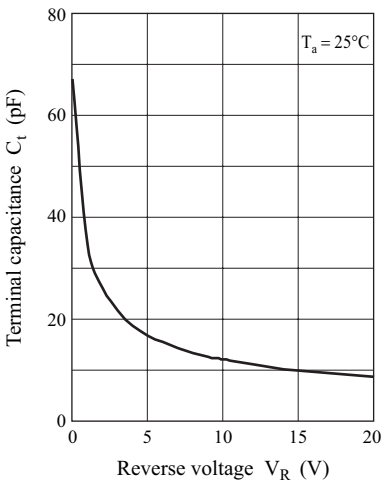
I_F — V_F



I_R — V_R



C_t — V_R



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