FG6K4206

Silicon N-channel MOS FET (FET1)
Silicon P-channel MOS FET (FET2)

For DC-DC converter circuits
For switching circuits

■ Overview

FG6K4206 is the dual-type MOS FET (N-channel and P-channel) which is the most suitable for DC-DC converter and other switching circuits.

■ Features

- N-channel + P-channel MOS FET in one package
- Low drain-source ON resistance: $R_{DS(on)}$ typ. =
  N-ch. : 2.0 Ω (V_{GS} = 4.0 V), P-ch. : 95 mΩ (V_{GS} = –4.0 V)
- Small size surface mounting package: WSMini6-F1-B (2.1 mm × 2.0 mm × 0.7 mm)
- 2.5 V drive
- Contributes to miniaturization of sets, mount area reduction
- Eco-friendly Halogen-free package

■ Packaging

FG6K42060L Embossed type (Thermo-compression sealing): 3000 pcs / reel (standard)

■ Absolute Maximum Ratings T_a = 25°C

Parameter		Symbol	Rating	Unit
FET1 (N-ch.)	Drain-source surrender voltage	V_{DSS}	30	V
	Gate-source surrender voltage	V_{GSS}	±12	V
	Drain current	I_D	100	mA
	Peak drain current	I_{DP}	200	mA
FET2 (P-ch.)	Drain-source surrender voltage	V_{DSS}	–20	V
	Gate-source surrender voltage	V_{GSS}	±10	V
	Drain current	I_D	–2	A
	Peak drain current	I_{DP}	–8	A
Overall	Total power dissipation *	P_D	700	mW
	Channel temperature	T_{ch}	150	°C
	Storage temperature	T_{stg}	–55 to +150	°C

Note) *: Measuring on ceramic substrate at 40 mm × 38 mm × 0.2 mm
P_D absolute maximum rating without a heat shink: 150 mW

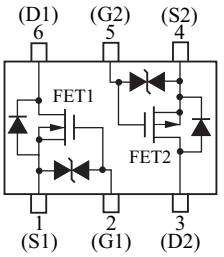
■ Package

- Code
  WSMini6-F1-B
  Package dimension clicks here.→ Click!

- Pin Name
  1. Source (FET1)
  2. Gate (FET1)
  3. Drain (FET2)
  4. Source (FET2)
  5. Gate (FET2)
  6. Drain (FET1)

■ Marking Symbol: Y7

■ Internal Connection



■ Electrical Characteristics T_a = 25°C±3°C

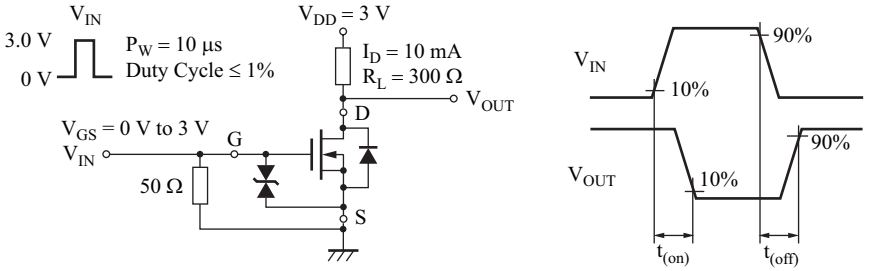
• FET1 (N-ch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = 1 mA, V_{GS} = 0	30			V
Drain-source cutoff current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0			1.0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0			±10	μA
Gate threshold voltage	V_{TH}	I_D = 1.0 μA, V_{DS} = 3.0 V	0.5	1	1.5	V
Drain-source ON resistance *1	$R_{DS(on)}$	I_D = 10 mA, V_{GS} = 2.5 V		3	6	Ω
		I_D = 10 mA, V_{GS} = 4.0 V		2	3	
Forward transfer admittance *1	$\lvert Y_{fs} \rvert$	I_D = 10 mA, V_{GS} = 3.0 V	20	55		mS
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} =3.0 V, V_{GS} = 0, f = 1 MHz		12		pF
Short-circuit output capacitance (Common source)	C_{oss}			7		pF
Reverse transfer capacitance (Common source)	C_{rss}			3		pF
Turn-on time *2	t_{on}	V_{DD} = 3.0 V, V_{GS} = 0 V to 3.0 V, I_D = 10 mA		100		ns
Turn-off time *2	t_{off}	V_{DD} = 3.0 V, V_{GS} = 3.0 V to 0 V, I_D = 10 mA		100		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *1: Pulse measurement

*2: Measurement circuit



■ Electrical Characteristics (continued) T_a = 25°C±3°C

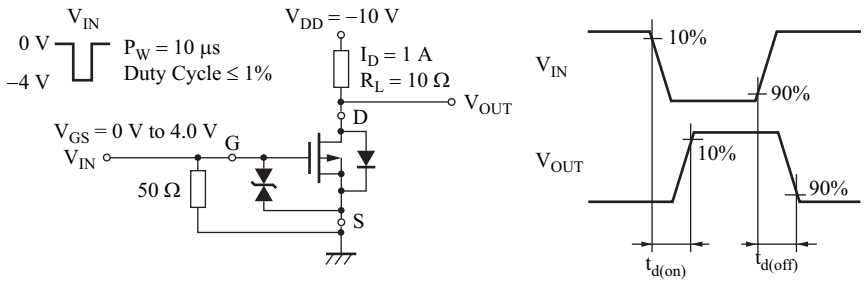
• FET2 (P-ch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = –1 mA, V_{GS} = 0	–20			V
Drain-source cutoff current	I_{DSS}	V_{DS} = –20 V, V_{GS} = 0			–1.0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±8 V, V_{DS} = 0			±10	μA
Gate threshold voltage	V_{TH}	I_D = –1.0 mA, V_{DS} = –10 V	– 0.4	– 0.75	–1.1	V
Drain-source ON resistance *1	$R_{DS(on)}$	I_D = – 0.5 A, V_{GS} = –1.8 V		155	245	mΩ
		I_D = –1 A, V_{GS} = –2.5 V		115	185	
		I_D = –1 A, V_{GS} = –4.0 V		95	135	
Forward transfer admittance *1	$\|Y_{fs}\|$	I_D = –1.0 A, V_{DS} = –10 V	3.0			S
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz		300		pF
Short-circuit output capacitance (Common source)	C_{oss}			30		pF
Reverse transfer capacitance (Common source)	C_{rss}			35		pF
Turn-on time *2	t_{on}	V_{DD} = –10 V, V_{GS} = 0 V to –4 V, I_D = –1.0 A		14		ns
Turn-off time *2	t_{off}	V_{DD} = –10 V, V_{GS} = –4 V to 0 V, I_D = –1.0 A		112		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

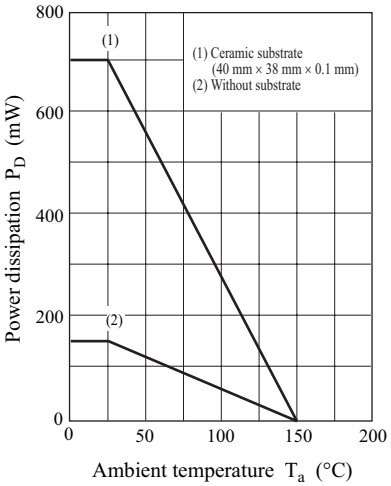
2. *1: Pulse measurement

*2: Measurement circuit



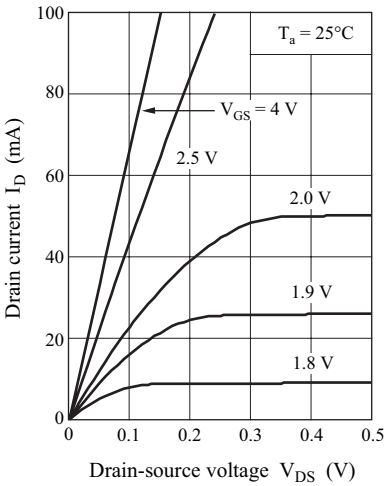
Common characteristics chart

P_D — T_a

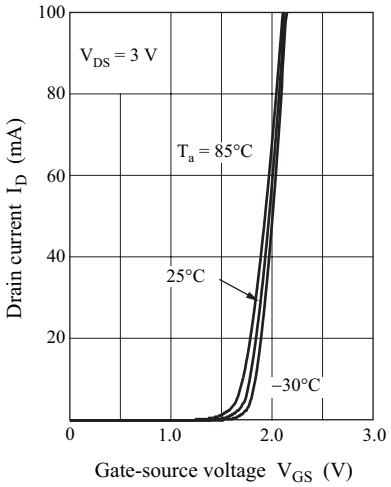


Characteristics charts of FET1

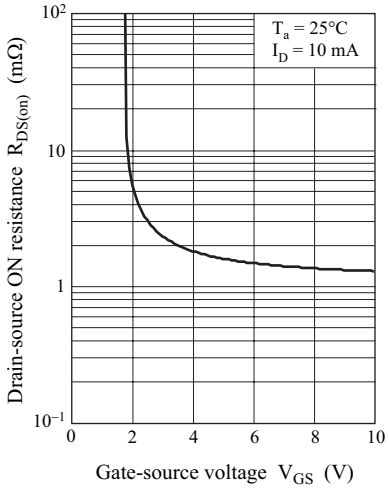
I_D — V_{DS}



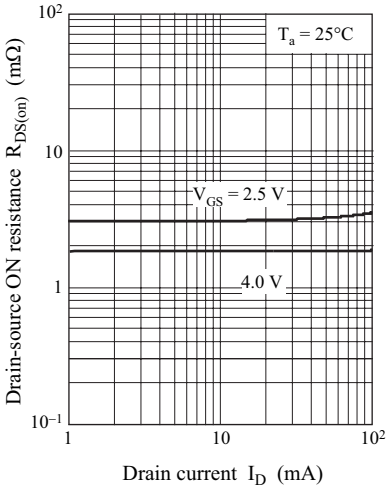
I_D — V_{GS}



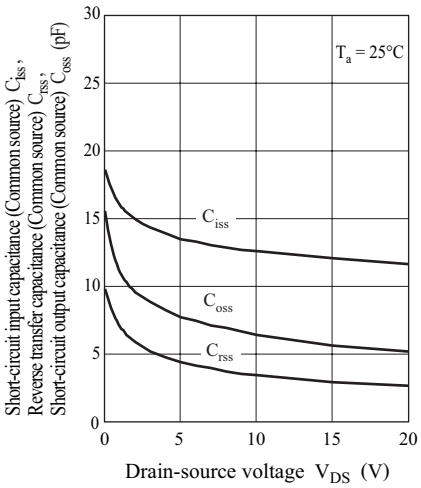
$R_{DS(on)}$ — V_{GS}



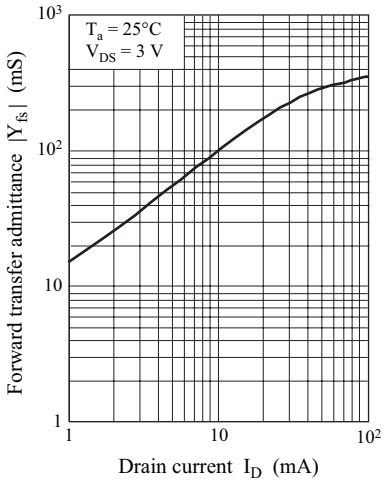
$R_{DS(on)}$ — I_D



C_{iss} , C_{rss} , C_{oss} — V_{DS}

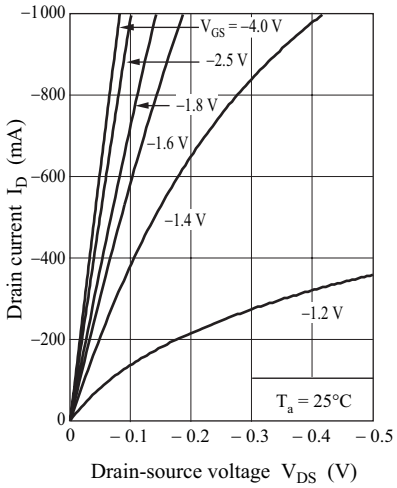


$|Y_{fs}|$ — I_D

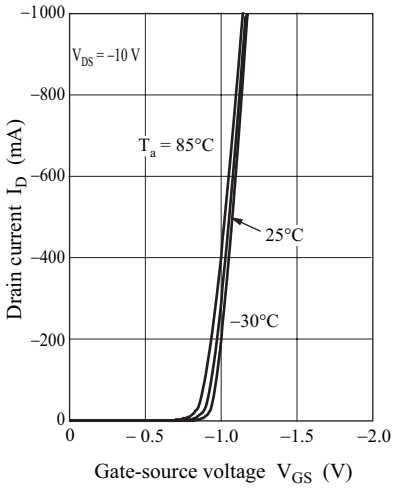


Characteristics charts of FET2

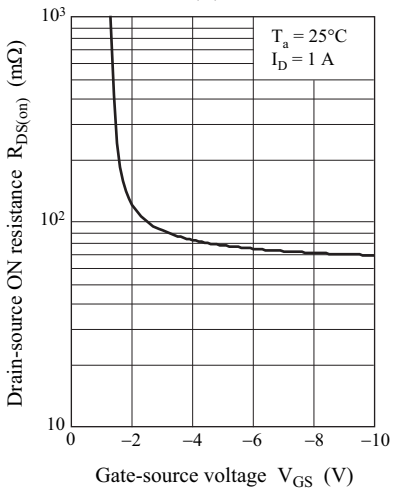
I_D — V_{DS}



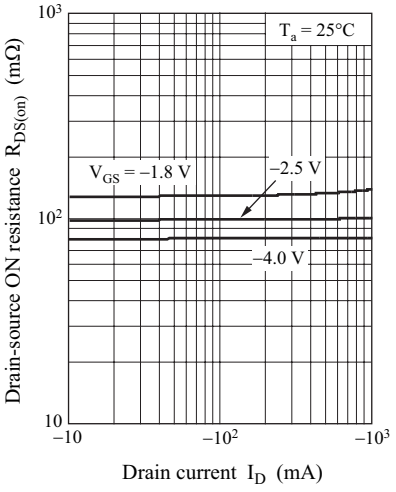
I_D — V_{GS}



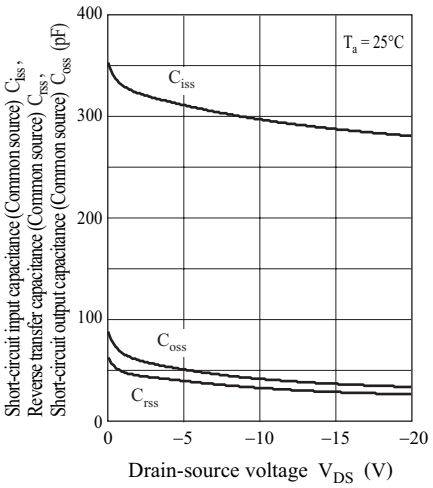
$R_{DS(on)}$ — V_{GS}



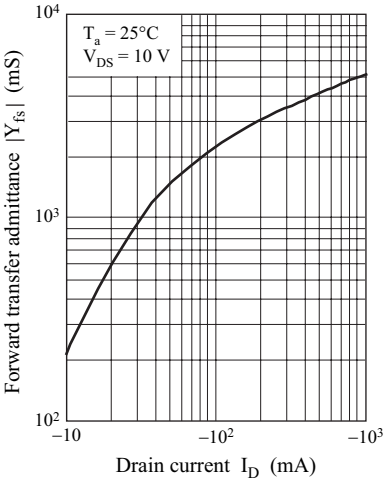
$R_{DS(on)}$ — I_D



C_{iss} , C_{rss} , C_{oss} — V_{DS}



$|Y_{fs}|$ — I_D



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