FG654301

Silicon N-channel MOS FET (FET1)
Silicon P-channel MOS FET (FET2)

For switching circuits

■ Overview

FG654301 is N-P channel dual type small signal MOS FET employed small size surface mounting package.

■ Features

- Low drain-source ON resistance:
  $R_{DS(on)}$ typ. = 2 Ω (V_{GS} = 4.0 V) / 4 Ω (V_{GS} = –4.0 V)
- High-speed switching
- Small size surface mounting package: SMini6-F3-B
- Contributes to miniaturization of sets, reduction of component count.
- Eco-friendly Halogen-free package

■ Packaging

FG6543010R Embossed type (Thermo-compression sealing): 8000 pcs / reel (standard)

■ Absolute Maximum Ratings T_a = 25°C

Parameter		Symbol	Rating	Unit
FET1	Drain-source surrender voltage	V_{DSS}	30	V
	Gate-source surrender voltage	V_{GSS}	±12	V
	Drain current	I_D	100	mA
	Peak drain current	I_{DP}	200	mA
FET2	Drain-source surrender voltage	V_{DSS}	–30	V
	Gate-source surrender voltage	V_{GSS}	±12	V
	Drain current	I_D	–100	mA
	Peak drain current	I_{DP}	–200	mA
Overall	Total power dissipation	P_T	150	mW
	Channel temperature	T_{ch}	150	°C
	Storage temperature	T_{stg}	–55 to +150	°C

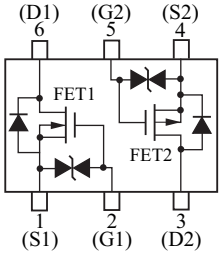
■ Package

- Code
  SMini6-F3-B
  Package dimension clicks here.→ Click!

- Pin Name
  1: Source (FET1) 4: Source (FET2)
  2: Gate (FET1) 5: Gate (FET2)
  3: Drain (FET2) 6: Drain (FET1)

■ Marking Symbol: V7

■ Internal Connection

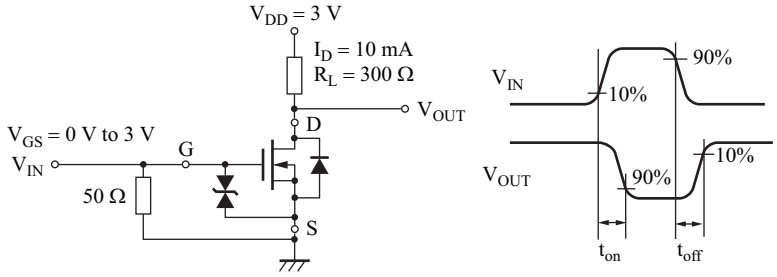


■ Electrical Characteristics T_a = 25°C±3°C

• FET1

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = 1 mA, V_{GS} = 0 V	30			V
Drain-source cutoff current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1.0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V			±10	μA
Gate threshold voltage	V_{TH}	I_D = 1.0 μA, V_{DS} = 3.0 V	0.5	1.0	1.5	V
Drain-source ON resistance	$R_{DS(on)}$	I_D = 10 mA, V_{GS} = 2.5 V		3	6	Ω
		I_D = 10 mA, V_{GS} = 4.0 V		2	3	
Forward transfer admittance	$\|Y_{fs}\|$	I_D = 10 mA, V_{DS} = 3.0 V	20	55		mS
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} = 3 V, V_{GS} = 0 V, f = 1 MHz		12		pF
Short-circuit output capacitance (Common source)	C_{oss}			7		pF
Reverse transfer capacitance (Common source)	C_{rss}			3		pF
Turn-on time *	t_{on}	V_{DD} = 3 V, V_{GS} = 0 V to 3 V, I_D = 10 mA		100		ns
Turn-off time *	t_{off}	V_{DD} = 3 V, V_{GS} = 3 V to 0 V, I_D = 10 mA		100		ns

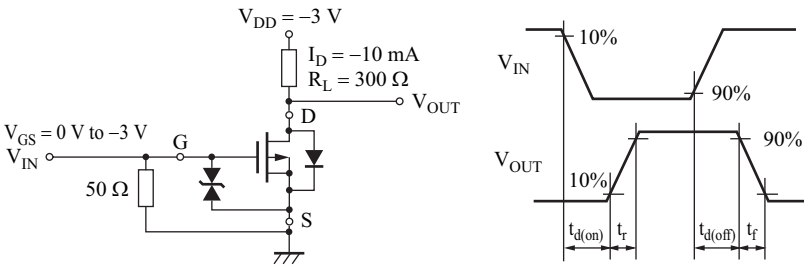
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *: Test circuit



• FET2

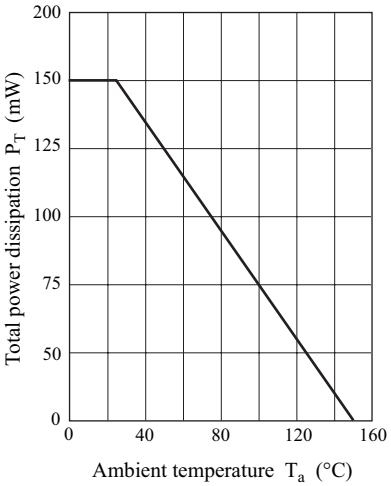
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	I_D = –1 mA, V_{GS} = 0 V	–30			V
Drain-source cutoff current	I_{DSS}	V_{DS} = –30 V, V_{GS} = 0 V			–1.0	μA
Gate-source cutoff current	I_{GSS}	V_{GS} = ±10 V, V_{DS} = 0 V			±10	μA
Gate threshold voltage	V_{TH}	I_D = –1.0 μA, V_{DS} = –3.0 V	– 0.5	–1.0	–1.5	V
Drain-source ON resistance	$R_{DS(on)}$	I_D = –10 mA, V_{GS} = –2.5 V		7	17	Ω
		I_D = –10 mA, V_{GS} = –4.0 V		4	7	
Forward transfer admittance	$\|Y_{fs}\|$	I_D = –10 mA, V_{DS} = –3.0 V	20	40		mS
Short-circuit input capacitance (Common source)	C_{iss}	V_{DS} = –3 V, V_{GS} = 0 V, f = 1 MHz		12		pF
Short-circuit output capacitance (Common source)	C_{oss}			7		pF
Reverse transfer capacitance (Common source)	C_{rss}			3		pF
Turn-on time *	t_{on}	V_{DD} = –3 V, V_{GS} = 0 V to –3 V, I_D = –10 mA		100		ns
Turn-off time *	t_{off}	V_{DD} = –3 V, V_{GS} = –3 V to 0 V, I_D = –10 mA		100		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
2. *: Test circuit



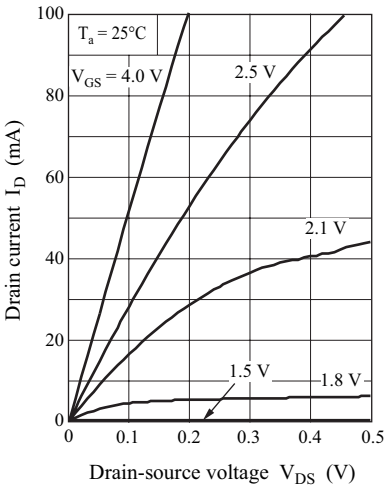
Common characteristics chart

P_T — T_a

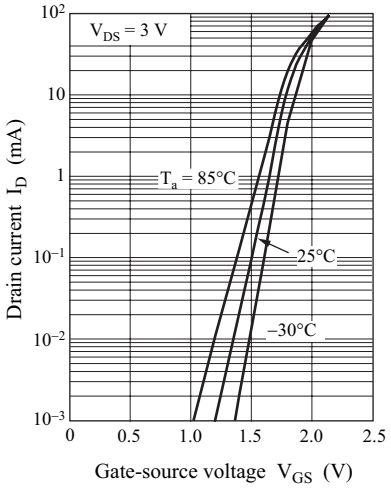


Characteristics charts of FET1

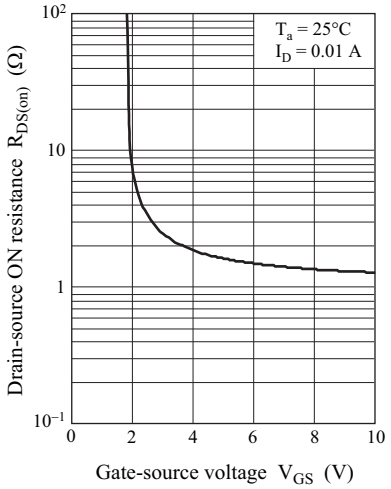
I_D — V_{DS}



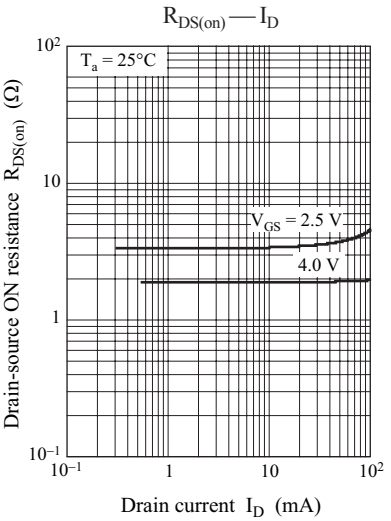
I_D — V_{GS}



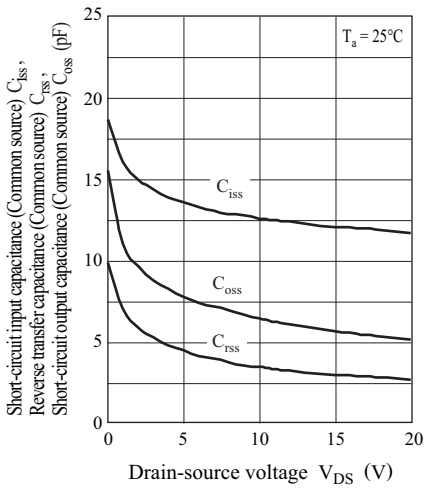
$R_{DS(on)}$ — V_{GS}



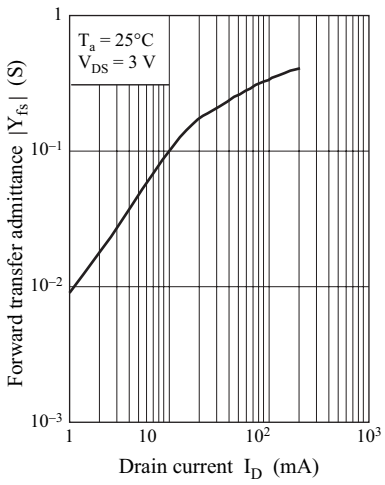
$R_{DS(on)}$ — I_D



C_{iss} , C_{rss} , C_{oss} — V_{DS}

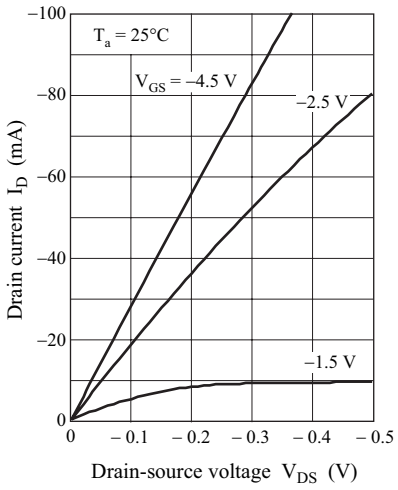


$|Y_{fs}|$ — I_D

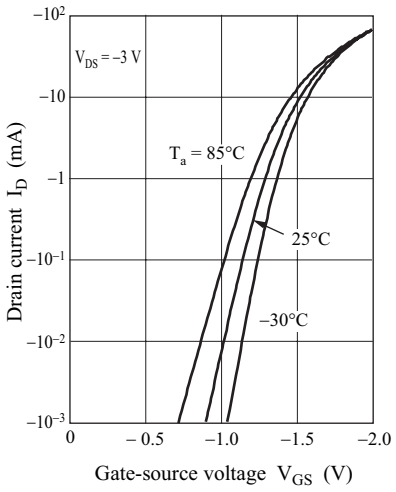


Characteristics charts of FET2

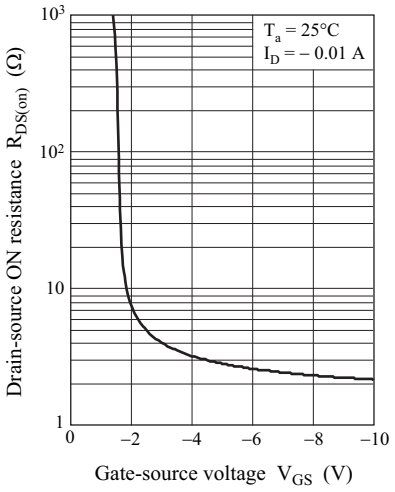
I_D — V_{DS}



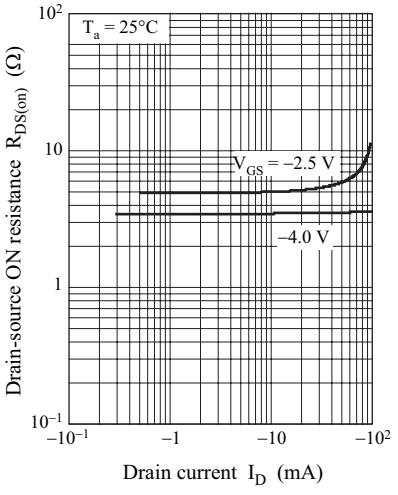
I_D — V_{GS}



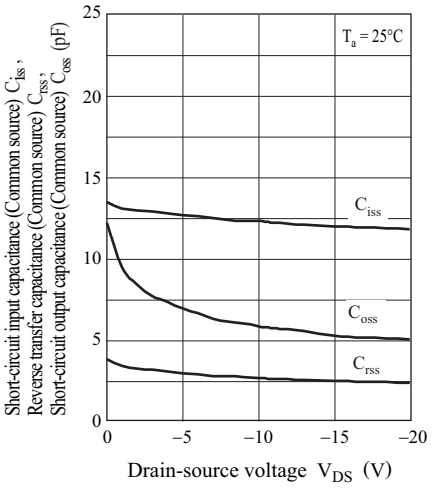
$R_{DS(on)}$ — V_{GS}



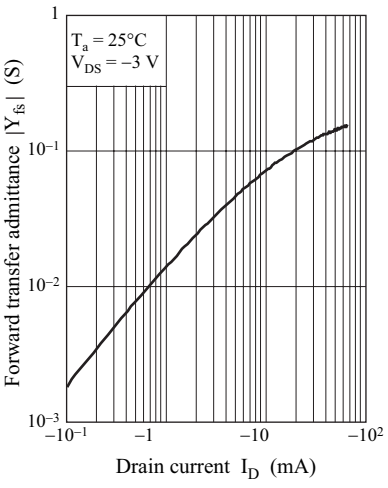
$R_{DS(on)}$ — I_D



C_{iss} , C_{rss} , C_{oss} — V_{DS}



$|Y_{fs}|$ — I_D



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