Silicon NPN Power Transistors 2SD1550

DESCRIPTION

·With TO-3P(H)IS package
·High voltage ,high speed
·Low collector saturation voltage

APPLICATIONS

·For color TV horizontal deflection output applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

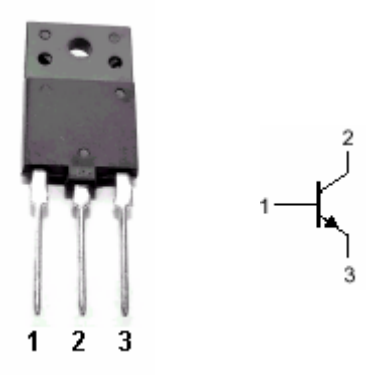

Fig.1 simplified outline (TO-3P(H)IS) and symbol

Absolute maximum ratings (Ta=25□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1000	V
V_{CEO}	Collector-emitter voltage	Open base	400	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		10	A
P_C	Collector power dissipation	T_C=25□	50	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{CEO(SUS)}$	Collector-emitter sustaining voltage	I_C=0.1A , I_B=0	400			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=8A ;I_B=1.6A			5.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C=8A ;I_B=1.6A			1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=800V; I_E=0			10	μA
I_{EBO}	Emitter cut-off current	V_{EB}=5V; I_C=0			10	μA
h_{FE-1}	DC current gain	I_C=1A ; V_{CE}=5V	8			
h_{FE-2}	DC current gain	I_C=8A ; V_{CE}=5V	5			

PACKAGE OUTLINE

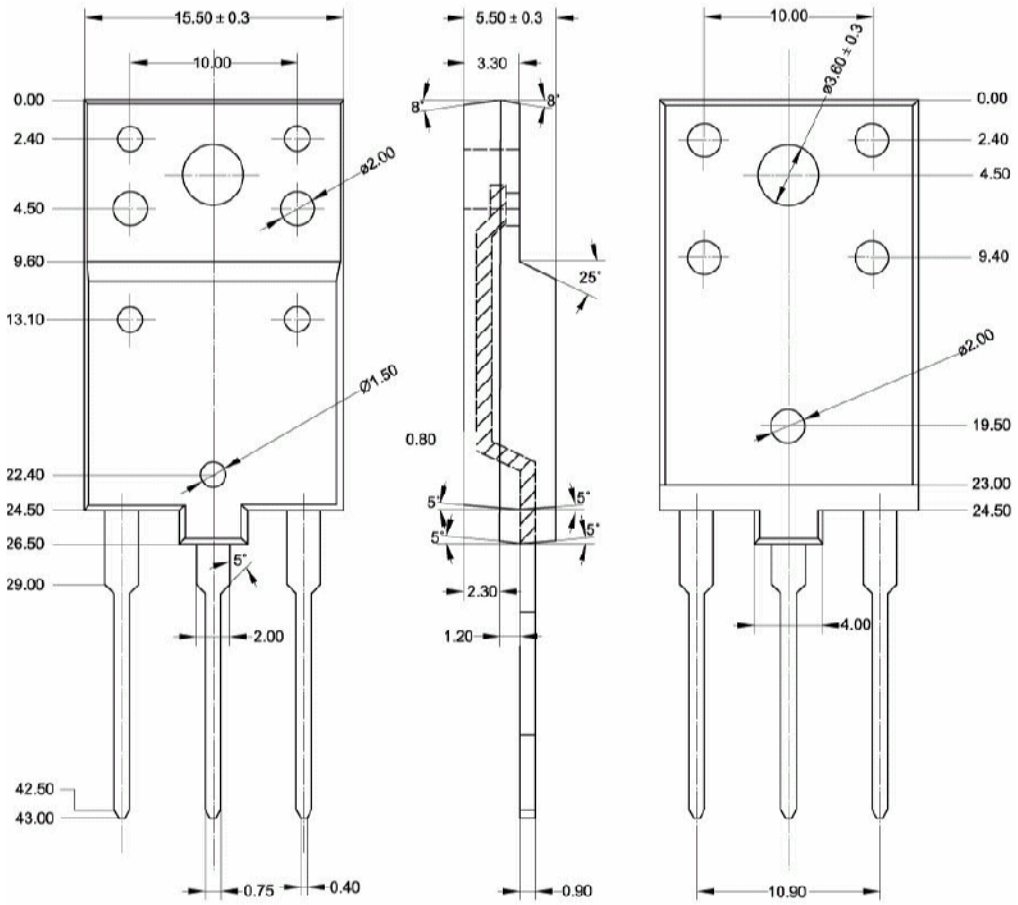

Fig.2 Outline dimensions (unindicated tolerance:±0.15 mm)