

Silicon NPN Power Transistors

2SC1893

DESCRIPTION

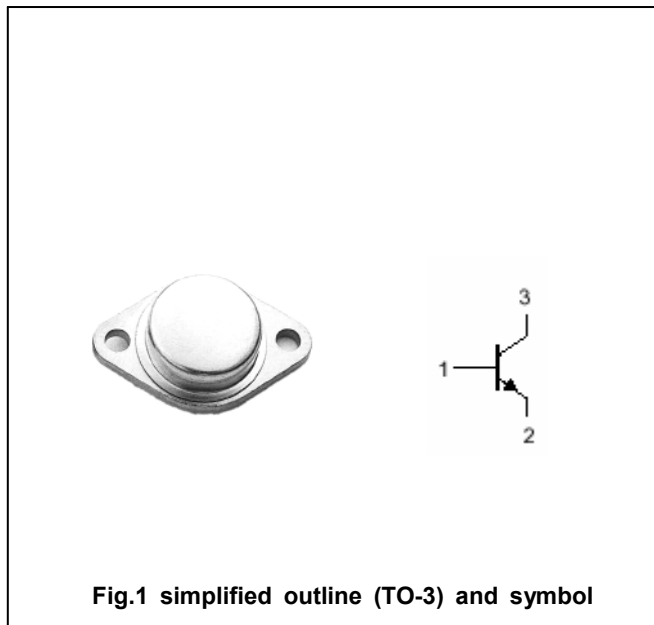
- With TO-3 package
- High breakdown voltage

APPLICATIONS

- For line-operated horizontal deflection output applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	500	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		3.5	A
P_C	Collector power dissipation	$T_C = 25 \square$	50	W
T_j	Junction temperature		150	\square
T_{stg}	Storage temperature		-55~150	\square

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	I _C =0.1A ; I _B =0	500			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =1mA ; I _C =0	5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =3A; I _B =0.6A			5.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =3A; I _B =0.6A			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =750V; I _E =0			50	μA
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			50	μA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =5V	10		40	
f _T	Transition frequency	I _C =0.1A ; V _{CE} =10V		3		MHz
C _{OB}	Collector output capacitance	I _E =0; V _{CB} =10V; f=1MHz		95		pF

PACKAGE OUTLINE



Fig.2 outline dimensions (unindicated tolerance:±0.1mm)