

Silicon PNP Power Transistors

2SB1551

DESCRIPTION

- With TO-220Fa package
- High DC current gain
- DARLINGTON

APPLICATIONS

- For medium speed and power switching applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector; connected to mounting base
3	Emitter

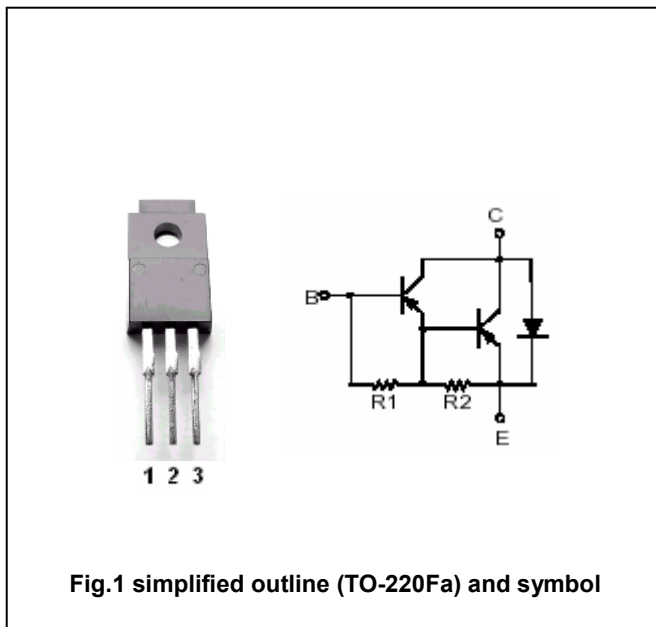


Fig.1 simplified outline (TO-220Fa) and symbol

Absolute maximum ratings(Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-80	V
V _{CEO}	Collector-emitter voltage	Open base	-80	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-10	A
P _C	Collector power dissipation	T _C =25°C	30	W
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-55~150	°C

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-10mA, I _B =0	-80			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-0.1mA, I _E =0	-80			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-2mA, I _C =0	-5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-5A, I _B =-20mA			-2.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-5A, I _B =-20mA			-2.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-80V, I _E =0			-10	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V, I _C =0			-2	mA
h _{FE}	DC current gain	I _C =-5A ; V _{CE} =-3V	1000		20000	

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PACKAGE OUTLINE

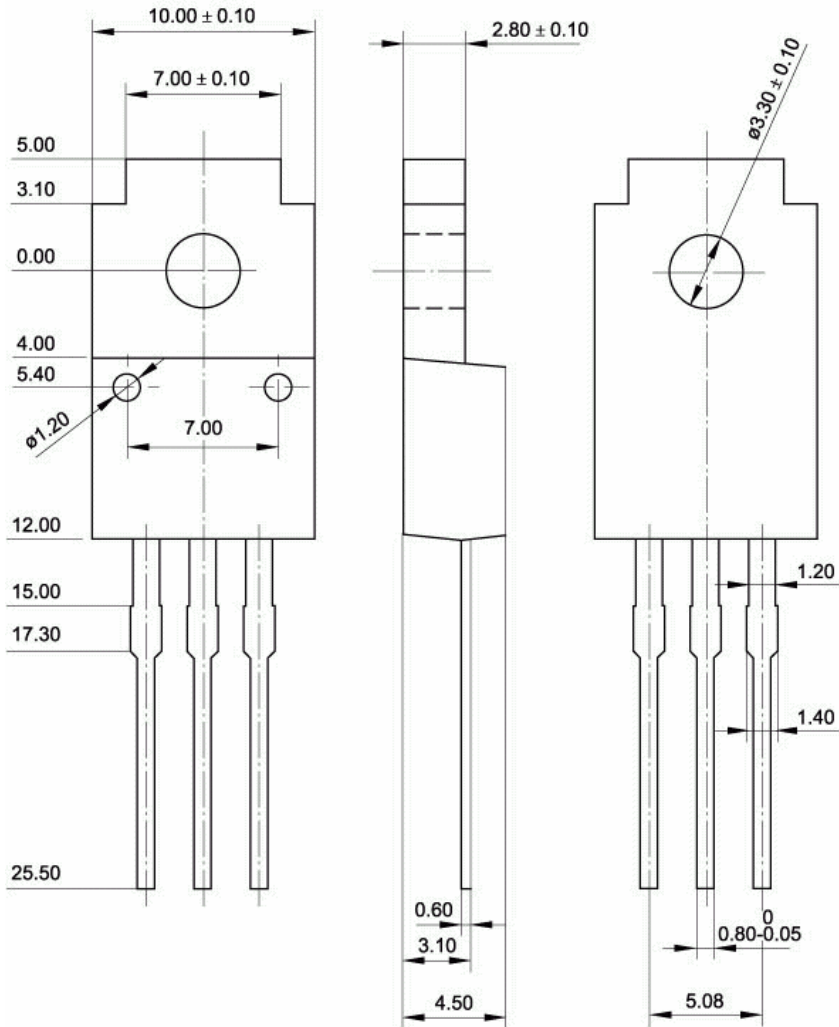


Fig.2 Outline dimensions (unindicated tolerance: ± 0.15 mm)