

Silicon PNP Power Transistors

2SB900

DESCRIPTION

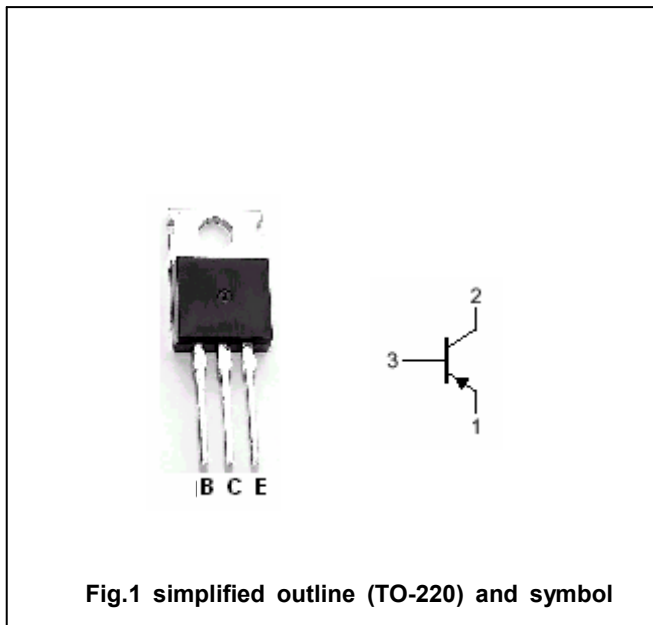
- With TO-220C package
- Low collector saturation voltage
- Wide area of safe operation

APPLICATIONS

- For power amplifier and switching applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



Absolute maximum ratings(Ta=25°C)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-50	V
V _{CEO}	Collector-emitter voltage	Open base	-50	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current (DC)		-4	A
P _C	Collector dissipation	T _C =25°C	40	W
T _j	Junction temperature		150	°C
T _{stg}	Storage temperature		-50~150	°C

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CHARACTERISTICS

T_j=25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-1mA; I _B =0	-50			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-1mA; I _E =0	-50			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA; I _C =0	-5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-2A; I _B =-0.2A			-1.0	V
V _{BE}	Base-emitter on voltage	I _C =-2A; V _{CE} =-4V			-1.4	V
I _{CBO}	Collector cut-off current	V _{CB} =-50V; I _E =0			-0.1	mA
I _{CEO}	Collector cut-off current	V _{CE} =-50V; I _E =0			-1.0	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-0.1	mA
h _{FE}	DC current gain	I _C =-1A; V _{CE} =-4V	40			

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PACKAGE OUTLINE



Fig.2 Outline dimensions (unindicated tolerance:±0.10mm)