Silicon PNP Power Transistors 2SB407

DESCRIPTION

·With TO-3 package
·Low collector saturation voltage
·Wide area of safe operation

APPLICATIONS

·For power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-30	V
V_{CEO}	Collector-emitter voltage	Open base	-30	V
V_{EBO}	Emitter-base voltage	Open collector	-10	V
I_C	Collector current		-7	A
P_C	Collector power dissipation	T_C=25□	30	W
T_j	Junction temperature		150	□
T_{stg}	Storage temperature		-55~150	□

Silicon PNP Power Transistors 2SB407

CHARACTERISTICS

Tj=25□ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	I_C=-10mA ;I_B=0	-30			V
$V_{(BR)CBO}$	Collector-base breakdown voltage	I_C=-1mA ;I_E=0	-30			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	I_E=-1mA ;I_C=0	-10			V
V_{CEsat}	Collector-emitter saturation voltage	I_C=-6A; I_B=-0.6A			-1.0	V
V_{BEsat}	Base-emitter saturation voltage	I_C=-6A; I_B=-0.6A			-1.5	V
I_{CBO}	Collector cut-off current	V_{CB}=-30V; I_E=0			-10	μA
I_{EBO}	Emitter cut-off current	V_{EB}=-10V; I_C=0			-10	μA
h_{FE}	DC current gain	I_C=-1A ; V_{CE}=-1.5V	80			

PACKAGE OUTLINE

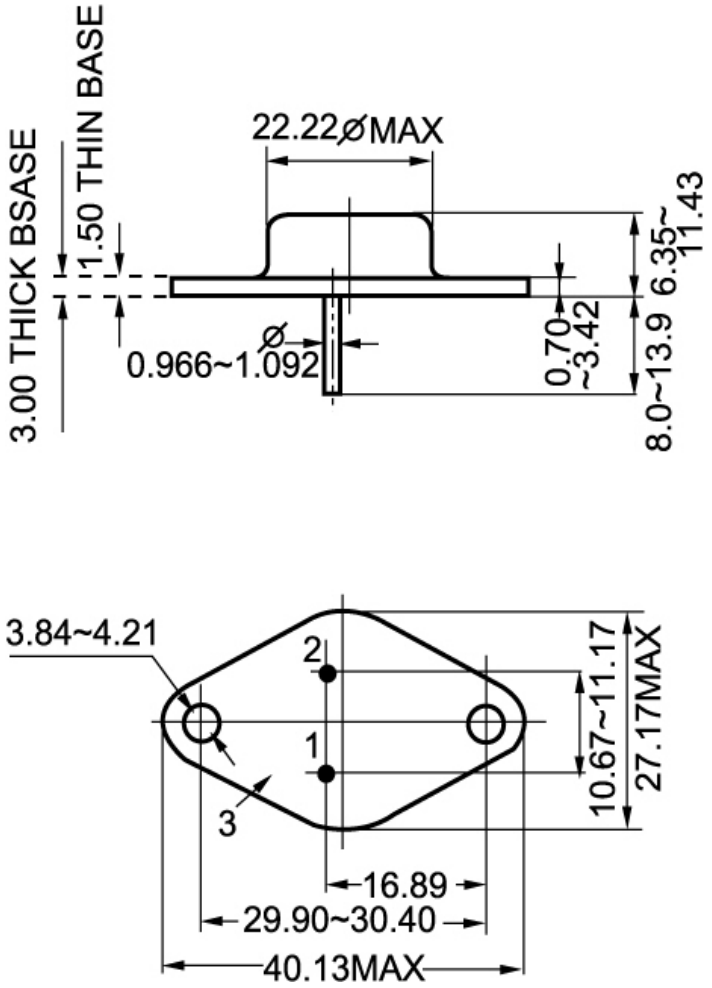

Fig.2 outline dimensions (unindicated tolerance:±0.1mm)