

Silicon PNP Power Transistors

2SA1180

DESCRIPTION

- With TO-3 package
- High power dissipations

APPLICATIONS

- For power switching amplifier and general purpose applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

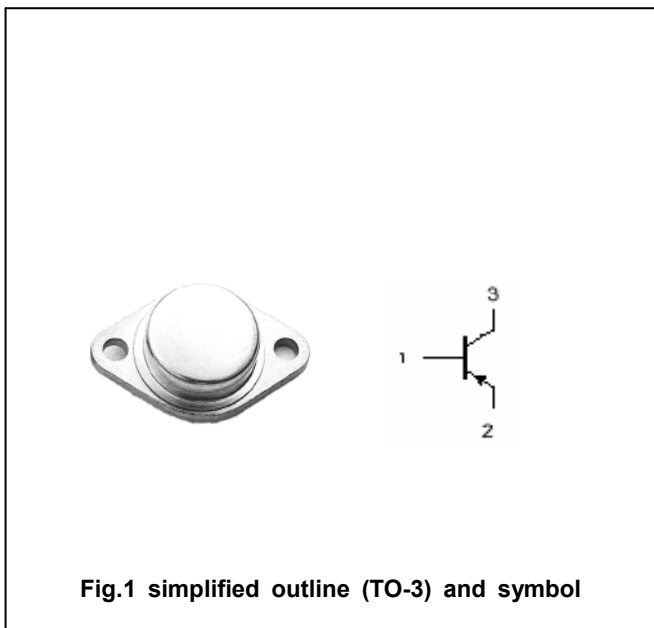


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-180	V
V _{CEO}	Collector-emitter voltage	Open base	-180	V
V _{EBO}	Emitter-base voltage	Open collector	-6	V
I _C	Collector current		-10	A
I _B	Base current		-4	A
P _C	Collector power dissipation	T _C =25□	100	W
T _j	Junction temperature		150	□
T _{stg}	Storage temperature		-55~150	□

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CHARACTERISTICS

Tj=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
$V_{(BR)CEO}$	Collector-emitter breakdown voltage	$I_C=-25mA ; I_B=0$	-180			V
$V_{(BR)CBO}$	Collector-base breakdown voltage	$I_C=-1mA ; I_E=0$	-180			V
$V_{(BR)EBO}$	Emitter-base breakdown voltage	$I_E=-1mA ; I_C=0$	-6			V
V_{CEsat}	Collector-emitter saturation voltage	$I_C=-5A ; I_B=-0.5A$			-2.0	V
V_{BEsat}	Base-emitter saturation voltage	$I_C=-5A ; I_B=-0.5A$			-2.5	V
I_{CBO}	Collector cut-off current	$V_{CB}=-180V ; I_E=0$			-0.1	mA
I_{EBO}	Emitter cut-off current	$V_{EB}=-6V ; I_C=0$			-0.1	mA
h_{FE}	DC current gain	$I_C=-5A ; V_{CE}=-4V$	30			

PACKAGE OUTLINE



Fig.2 outline dimensions (unindicated tolerance:±0.1mm)