

Silicon PNP Power Transistors

2N6594

DESCRIPTION

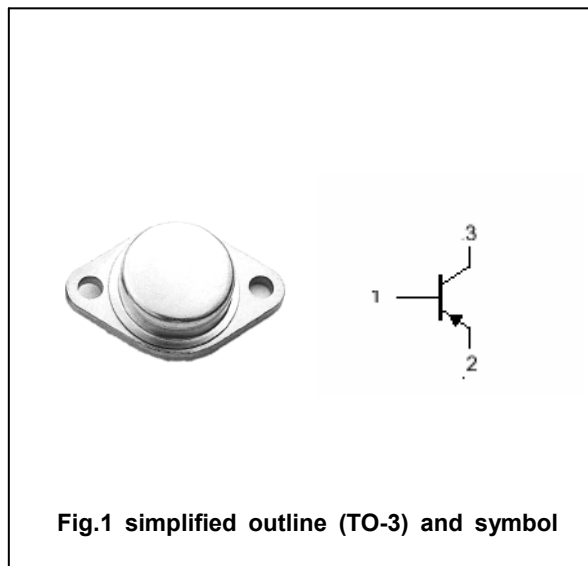
- With TO-3 package
- Complement to type 2N6569
- Wide area of safe operation

APPLICATIONS

- Designed for low voltage amplifier power switching applications

PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector



Absolute maximum ratings(Ta=□)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V <sub>CBO</sub>	Collector-base voltage	Open emitter	-45	V
V <sub>CEO</sub>	Collector-emitter voltage	Open base	-40	V
V <sub>EBO</sub>	Emitter-base voltage	Open collector	-5	V
I <sub>C</sub>	Collector current		-12	A
I <sub>CM</sub>	Collector current-peak		-24	A
I <sub>B</sub>	Base current		-5	A
I <sub>E</sub>	Emitter current		-17	A
I <sub>EM</sub>	Emitter current-peak		-34	A
P <sub>C</sub>	Collector power dissipation	T <sub>C</sub> =25□	100	W
T <sub>j</sub>	Junction temperature		200	□
T <sub>stg</sub>	Storage temperature		-65~200	□

## Silicon PNP Power Transistors

## 2N6594

## CHARACTERISTICS

T<sub>j</sub>=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>CEO(SUS)</sub>	Collector-emitter sustaining voltage	I <sub>C</sub> =-0.1A ; I <sub>B</sub> =0	-40			V
V <sub>CEsat-1</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =-4A; I <sub>B</sub> =-0.4A			-1.5	V
V <sub>CEsat-2</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =-12A; I <sub>B</sub> =-2.4A			-4.0	V
V <sub>BEsat</sub>	Base-emitter saturation voltage	I <sub>C</sub> =-4A; I <sub>B</sub> =-0.4A			-2.0	V
I <sub>CEO</sub>	Collector cut-off current	V <sub>CE</sub> =-40V; I <sub>B</sub> =0			-1.0	mA
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =-45V; I <sub>E</sub> =0			-1.0	mA
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =-5V; I <sub>C</sub> =0			-5.0	mA
h <sub>FE-1</sub>	DC current gain	I <sub>C</sub> =-4A ; V <sub>CE</sub> =-3V	15		200	
h <sub>FE-2</sub>	DC current gain	I <sub>C</sub> =-12A ; V <sub>CE</sub> =-4V	5		100	
f <sub>T</sub>	Transition frequency	I <sub>C</sub> =-1.0A ; V <sub>CE</sub> =-4V; f=0.5MHz	1.5		20	MHz

## Switching times

t <sub>d</sub>	Delay time	I <sub>C</sub> =-2A; I <sub>B1</sub> =-I <sub>B2</sub> =-0.2A V <sub>CC</sub> =-30V; t <sub>p</sub> =25μs; Duty Cycle≤2.0%			0.4	μs
t <sub>r</sub>	Rise time				1.5	μs
t <sub>stg</sub>	Storage time				5.0	μs
t <sub>f</sub>	Fall time				1.5	μs

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R <sub>th j-c</sub>	Thermal resistance junction to case	1.75	°C/W

Silicon PNP Power Transistors

2N6594

PACKAGE OUTLINE



Fig.2 outline dimensions (unindicated tolerance:±0.1mm)