Normally – OFF Silicon Carbide Junction Transistor

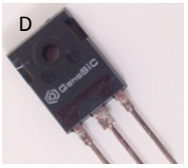
V_{DS}	=	1200 V
$V_{DS(ON)}$	=	1.4 V
I_D	=	50 A
$R_{DS(ON)}$	=	28 mΩ

Features

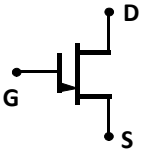
- 175 °C maximum operating temperature
- Temperature independent switching performance
- Gate oxide free SiC switch
- Suitable for connecting an anti-parallel diode
- Positive temperature coefficient for easy paralleling
- Low gate charge
- Low intrinsic capacitance

Package

- RoHS Compliant



TO-247AB



Advantages

- SiC transistor most compatible with existing Si gate-drivers
- Low switching losses
- Higher efficiency
- High temperature operation
- High short circuit withstand capability

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Values	Unit
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	1200	V
Continuous Drain Current	I_D	$T_{C,MAX}$ = 95 °C	50	A
Gate Peak Current	I_{GM}		10	A
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 175 °C, I_G = 1 A, Clamped Inductive Load	$I_{D,max}$ = 50 @ $V_{DS} \le V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 175 °C, I_G = 1 A, V_{DS} = 800 V, Non Repetitive	20	µs
Reverse Gate – Source Voltage	V_{SG}		30	V
Reverse Drain – Source Voltage	V_{SD}		25	V
Power Dissipation	P_{tot}	T_C = 95 °C	308	W
Storage Temperature	T_{stg}		-55 to 175	°C

Electrical Characteristics

Parameter	Symbol	Conditions	Values min.	Values typ.	Values max.	Unit
On Characteristics						
Drain – Source On Voltage	$V_{DS(ON)}$	I_D = 50 A, I_G = 1000 mA, T_j = 25 °C		1.4		V
		I_D = 50 A, I_G = 2000 mA, T_j = 125 °C		1.6		
		I_D = 50 A, I_G = 4000 mA, T_j = 175 °C		2.2		
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 50 A, I_G = 1000 mA, T_j = 25 °C		28		mΩ
		I_D = 50 A, I_G = 2000 mA, T_j = 125 °C		32		
		I_D = 50 A, I_G = 4000 mA, T_j = 175 °C		44		
Gate Forward Voltage	$V_{GS(FWD)}$	I_G = 500 mA, T_j = 25 °C		3.3		V
		I_G = 500 mA, T_j = 175 °C		3.1		
DC Current Gain	β	V_{DS} = 5 V, I_D = 50 A, T_j = 25 °C		TBD		
		V_{DS} = 5 V, I_D = 50 A, T_j = 175 °C		TBD		
Off Characteristics						
Drain Leakage Current	I_{DSS}	V_R = 1200 V, V_{GS} = 0 V, T_j = 25 °C		18		µA
		V_R = 1200 V, V_{GS} = 0 V, T_j = 125 °C		26		
		V_R = 1200 V, V_{GS} = 0 V, T_j = 175 °C		35		
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Capacitance Characteristics						
Gate-Source Capacitance	C_{gs}	V_{GS} = 0 V, f = 1 MHz		tbd		pF
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_D = 1 V, f = 1 MHz		tbd		pF
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	V_D = 1 V, f = 1 MHz		tbd		pF
Switching Characteristics						
Turn On Delay Time	$t_{d(on)}$	T_j = 25 ºC, V_{DS} = 800 V, I_D = 50 A, Two-Level Gate Drive, R_G = 1.5 Ω, C_G = 32 nF, V_{GH} = 18 V, V_{GL} = 6.5 V, V_{EE} = -10 V, IXDD614 Gate Drive IC, L = 287 µH, FWD = GB50SLT12, Refer to Fig. 15 for gate current waveform		tbd		ns
Rise Time	t_r			tbd		ns
Turn Off Delay Time	$t_{d(off)}$			tbd		ns
Fall Time	t_f			tbd		ns
Turn-On Energy Per Pulse	E_{on}			tbd		µJ
Turn-Off Energy Per Pulse	E_{off}			tbd		µJ
Total Switching Energy	E_{ts}			tbd		µJ
Turn On Delay Time	$t_{d(on)}$	T_j = 175 ºC, V_{DS} = 800 V, I_D = 50 A, Two-Level Gate Drive, R_G = 1.5 Ω, C_G = 32 nF, V_{GH} = 18 V, V_{GL} = 6.5 V, V_{EE} = -10 V, IXDD614 Gate Drive IC, L = 287 µH, FWD = GB50SLT12, Refer to Fig. 15 for gate current waveform		tbd		
Rise Time	t_r			tbd		ns
Turn Off Delay Time	$t_{d(off)}$			tbd		ns
Fall Time	t_f			tbd		ns
Turn-On Energy Per Pulse	E_{on}			tbd		µJ
Turn-Off Energy Per Pulse	E_{off}			tbd		µJ
Total Switching Energy	E_{ts}			tbd		µJ
Thermal Characteristics						
Thermal resistance, junction - case	R_{thJC}			0.26		°C/W

Figures

TBD

Figure 1: Typical Output Characteristics at 25 °C

TBD

Figure 2: Typical Output Characteristics at 125 °C

Figure 3: Typical Output Characteristics at 175 °C

Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

Figure 6: Typical Blocking Characteristics

Figure 7: Capacitance Characteristics

Figure 8: Capacitance Characteristics

Figure 9: Typical Hard-switched Turn On Waveforms

Figure 10: Typical Hard-switched Turn Off Waveforms

Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

Figure 13: Typical Turn On Energy Losses vs. Drain Current

Figure 14: Typical Turn Off Energy Losses vs. Drain Current

Figure 15: Typical Gate Current Waveform

Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency [1]

Figure 17: Power Derating Curve

Figure 18: Forward Bias Safe Operating Area

Figure 19: Turn-Off Safe Operating Area

Figure 20: Transient Thermal Impedance

[1] – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

Commercial Gate Drivers Compatible with GA50JT12-247

Manufacturer	Part Number	Peak Current Output	Features: Optical Signal Isolation	Features: Desaturation Detection	Features: Under Voltage Lockout	Features: Active Miller Clamping
Avago Tech.	HCPL-316J	2.5	✓	✓	✓	–
Avago Tech.	HCPL-322J	2.5	✓	✓	✓	✓
IXYS	IXD_604	4.0	–	–	–	–
IXYS	IXD_609	9.0	–	–	–	–
IXYS	IXD_614	14.0	–	–	–	–
IXYS	IXD_630	30.0	–	–	–	–
IXYS	IRFD630	30.0	–	–	–	–
Micrel	MIC4452YN	12.0	–	–	–	–
Microsemi	LX1780QLQ	15.0	–	–	✓	–
Texas Instruments	UCC27322	9.0	–	–	–	–

This is a partial list of widely available commercial Silicon IGBT/MOSFET gate drivers which may be used to drive the GA50JT12-247. Specific product information including advanced features and pinouts should be obtained from the individual product manufacturer's websites.

The gate of the GA50JT12-247 can be driven similar to a silicon IGBT or MOSFET in which a gate driver IC is used to supply positive gate current peaks to the device at turn-on and negative current peaks at turn-off. Unlike the IGBT or MOSFET, the GA50JT12-247 also requires a continuous gate current for the device to remain on after the initial current peak. An example gate current waveform for the GA50JT12-247 can be seen in Fig. 15.

Single-Level SJT Gate Drive

Producing the necessary gate current peaks and continuous currents can be done very simply using a circuit similar what is shown in Fig. 21 in which an external gate capacitor and resistor are placed in parallel connected to the gate drive output node and the SJT gate. The gate resistor is chosen to control the continuous gate current and adjusting the external capacitance will alter positive and negative current peaks. More details can be found in a series of GeneSiC Semiconductor Application Notes. (http://www.genesicsemi.com/index.php/references/notes)

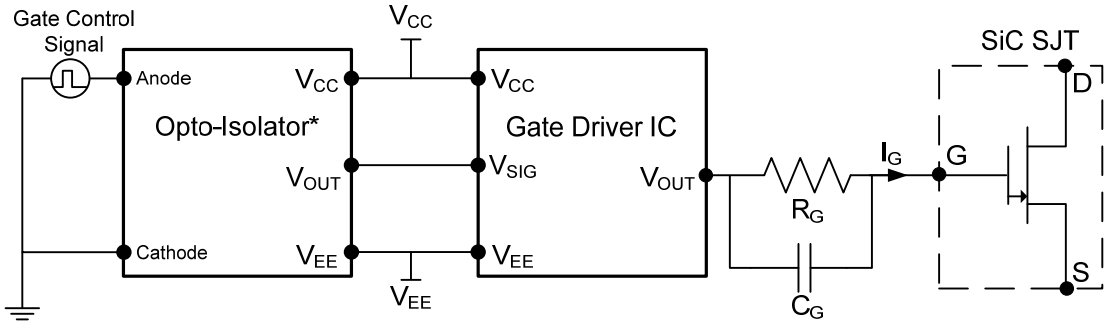


Figure 21: Single-Level SJT Gate Diver Configuration (* – External signal isolation is required for non-isolated gate driver ICs.)

Single-Level Gate Drive Conditions

Parameter	Symbol	Conditions	Values: Min.	Values: Optimum	Values: Max.	Unit
Supply Voltage	V_{CC}		10	tbd		V
Negative Supply Voltage	V_{EE}		-10	tbd	GND	V
Output Current, Peak	$I_{OUT, pk}$	Package Limited,	2.0	tbd		A
Output Current, Continuous	I_{OUT}	T = 175 °C	0.7	tbd		A
Output Gate Components						
Gate Resistance	R_G	V_{CC} = 20 V, I_G ≈ 1.0 A, T = 175 °C	15	tbd		Ω
Gate Capacitance	C_G	V_{CC} = 20 V $I_{G,pk}$ ≈ 4.0 A, T = 175 °C	20	tbd		nF

Two-Level SJT Gate Drive

The gate of the GA50JT12-247 can also be driven with a slightly more advanced gate drive circuit, seen in Fig. 22, in which two gate drive ICs are used with two different supply voltage (V_{CC}) levels in order to minimize gate drive losses. By using a second, lower voltage output gate driver IC the power consumption of the continuous current is reduced. Additional detail on this Two-Level SJT gate driving technique is discussed in GeneSiC Semiconductor Application Note AN-10B. (http://www.genesicsemi.com/index.php/references/notes)

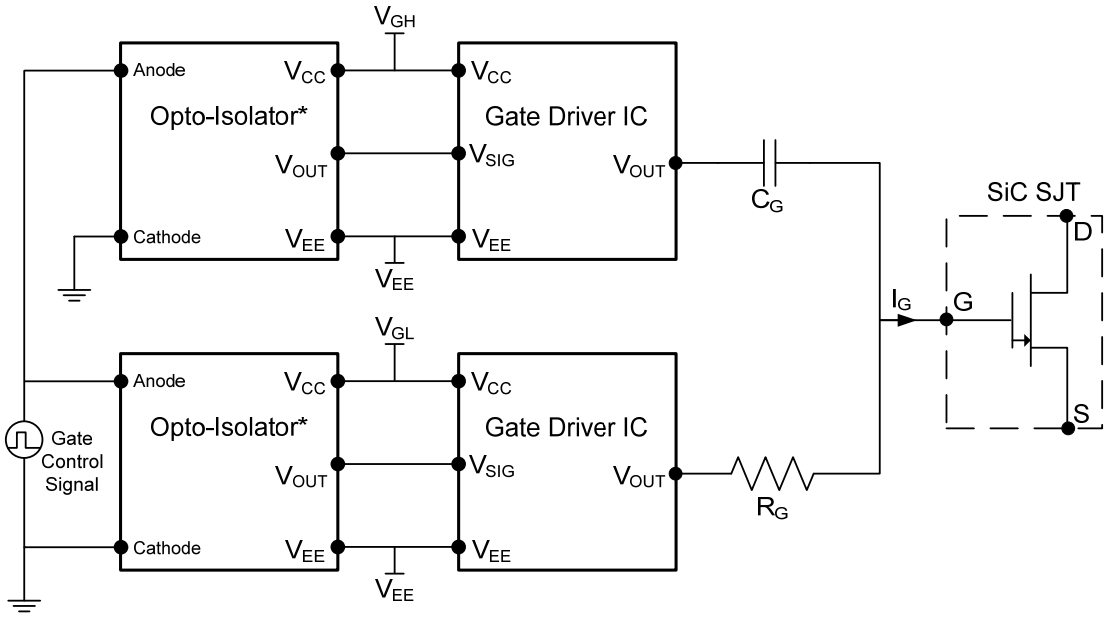


Figure 22: Two-Level SJT Gate Diver Configuration for Reduced Drive Losses (* – External signal isolation is required for non-isolated gate driver ICs.)

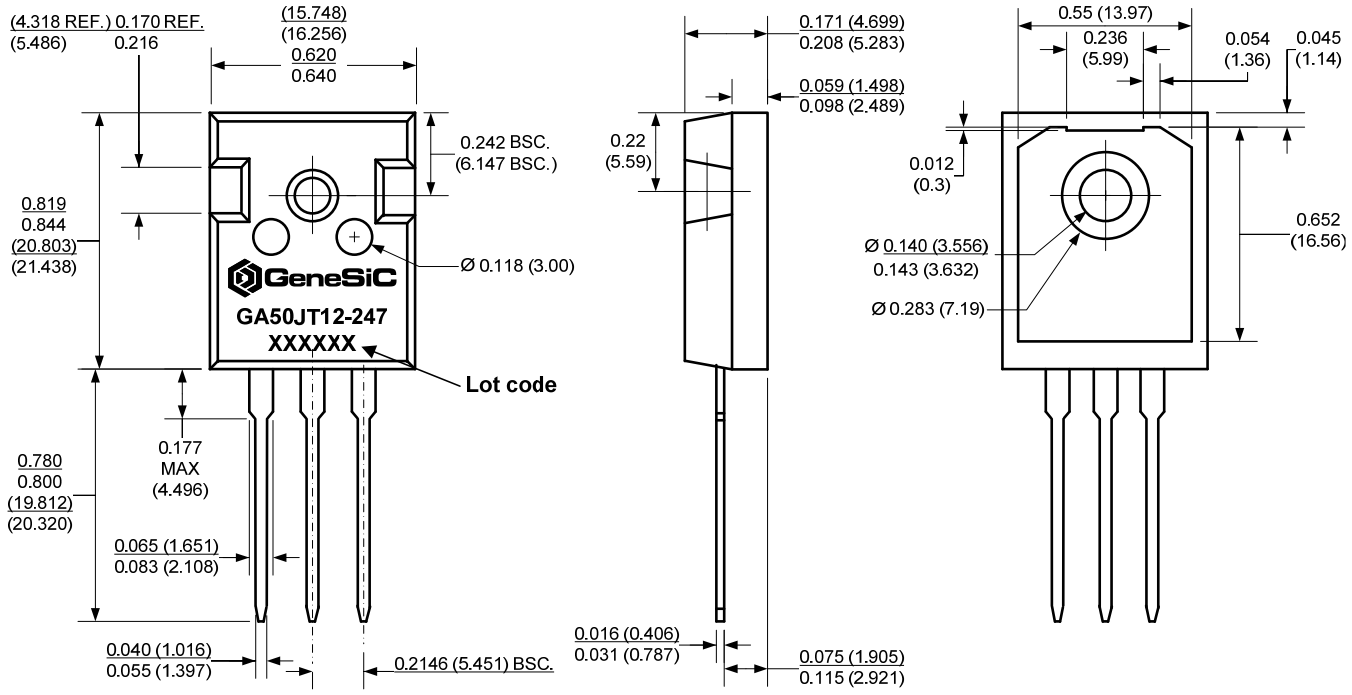
Two-Level Gate Drive Conditions

Parameter	Symbol	Conditions	Values			Unit
			min.	Optimum	max.	
Supply Voltage, High Level Driver	V_{CC} (V_{GH}+)		15	tbd		V
Supply Voltage, Low Level Driver	V_{CC}(V_{GL}+)		5	tbd		V
Negative Supply Voltage	V_{EE}			tbd	GND	V
Output Current, Peak	I_{OUT}	Package Limited	2.0	tbd		A
Output Current, Continuous	I_{OUT}	T = 175 °C	0.7	tbd		A
Output Gate Components						
Gate Resistance	R_G	V_{GL} = 6.5 V, I_G ≈ 1.0 A, T = 175 °C		tbd	4	Ω
Gate Capacitance	C_G	V_{GH} = 20 V, $I_{G,pk}$ ≈ 4.0 A, T = 175 °C	20	tbd		nF

+ – Consult application note AN-10B for more information on parameters V_{GH} and V_{GL}.

Package Dimensions:

TO-247AB **PACKAGE OUTLINE**



NOTE
1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2013/12/18	1	Updated Gate Drive Section	
2013/09/12	0	Initial release	

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SPICE Model Parameters

This is a secure document. Copy this code from the SPICE model PDF file on our website into a SPICE software program for simulation of the GA50JT12.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   1.0           $
*     $Date:   12-SEP-2013       $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
*     COPYRIGHT (C) 2013 GeneSiC Semiconductor Inc.
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*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model GA50JT12 NPN
+ IS       5.00E-47
+ ISE      1.26E-28
+ EG       3.2
+ BF       100
+ BR       0.55
+ IKF      3500
+ NF       1
+ NE       2
+ RB       0.26
+ RE       0.01
+ RC       0.011
+ CJC      1.75E-9
+ VJC      3
+ MJC      0.5
+ CJE      5.57E-9
+ VJE      3
+ MJE      0.5
+ XTI      3
+ XTB      -1.2
+ TRC1     7.00E-3
+ VCEO     1200
+ ICRATING 50
+ MFG      GeneSiC_Semiconductor
*
* End of GA50JT12 SPICE Model
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