

## Normally – OFF Silicon Carbide Junction Transistor

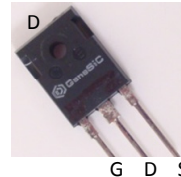
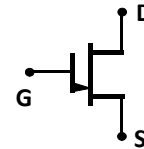
$V_{DS}$	=	<b>1200 V</b>
$V_{DS(ON)}$	=	<b>1.4 V</b>
$I_D$	=	<b>5 A</b>
$R_{DS(ON)}$	=	<b>280 mΩ</b>

### Features

- 175 °C maximum operating temperature
- Temperature independent switching performance
- Gate oxide free SiC switch
- Suitable for connecting an anti-parallel diode
- Positive temperature coefficient for easy paralleling
- Low gate charge
- Low intrinsic capacitance

### Package

- RoHS Compliant


**TO-247AB**


### Advantages

- SiC transistor most compatible with existing Si gate-drivers
- Low switching losses
- Higher efficiency
- High temperature operation
- High short circuit withstand capability

### Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

### Absolute Maximum Ratings

Parameter	Symbol	Conditions	Values	Unit
Drain – Source Voltage	$V_{DS}$	$V_{GS} = 0 V$	1200	V
Continuous Drain Current	$I_D$	$T_{C,MAX} = 95\text{ °C}$	5	A
Gate Peak Current	$I_{GM}$		5	A
Reverse Gate – Source Voltage	$V_{SG}$		30	V
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 175\text{ °C}$ , $I_G = 1 A$ , Clamped Inductive Load	$I_{D,max} = 5$ @ $V_{DS} \leq V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 175\text{ °C}$ , $I_G = 1 A$ , $V_{DS} = 800 V$ , Non Repetitive	20	$\mu s$
Reverse Drain – Source Voltage	$V_{SD}$		25	V
Power Dissipation	$P_{tot}$	$T_C = 95\text{ °C}$	57	W
Storage Temperature	$T_{stg}$		-55 to 175	°C

### Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>On Characteristics</b>						
Drain – Source On Voltage	$V_{DS(ON)}$	$I_D = 5 A$ , $I_G = 100 mA$ , $T_J = 25\text{ °C}$		1.4		V
		$I_D = 5 A$ , $I_G = 200 mA$ , $T_J = 125\text{ °C}$		1.6		
		$I_D = 5 A$ , $I_G = 400 mA$ , $T_J = 175\text{ °C}$		2.2		
Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 5 A$ , $I_G = 100 mA$ , $T_J = 25\text{ °C}$		280		mΩ
		$I_D = 5 A$ , $I_G = 200 mA$ , $T_J = 125\text{ °C}$		320		
		$I_D = 5 A$ , $I_G = 400 mA$ , $T_J = 175\text{ °C}$		440		
Gate Forward Voltage	$V_{GS(FWD)}$	$I_G = 500 mA$ , $T_J = 25\text{ °C}$ $I_G = 500 mA$ , $T_J = 175\text{ °C}$		3.3 3.1		V
DC Current Gain	$\beta$	$V_{DS} = 5 V$ , $I_D = 5 A$ , $T_J = 25\text{ °C}$		TBD		
		$V_{DS} = 5 V$ , $I_D = 5 A$ , $T_J = 175\text{ °C}$		TBD		
<b>Off Characteristics</b>						
Drain Leakage Current	$I_{DSS}$	$V_R = 1200 V$ , $V_{GS} = 0 V$ , $T_J = 25\text{ °C}$		210		nA
		$V_R = 1200 V$ , $V_{GS} = 0 V$ , $T_J = 125\text{ °C}$		310		
		$V_R = 1200 V$ , $V_{GS} = 0 V$ , $T_J = 175\text{ °C}$		420		
Gate Leakage Current	$I_{SG}$	$V_{SG} = 20 V$ , $T_J = 25\text{ °C}$		20		nA

**Electrical Characteristics**

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Capacitance Characteristics</b>						
Gate-Source Capacitance	$C_{GS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		tbd		pF
Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, V_D = 1\text{ V}, f = 1\text{ MHz}$		tbd		pF
Reverse Transfer/Output Capacitance	$C_{RSS}/C_{OSS}$	$V_D = 1\text{ V}, f = 1\text{ MHz}$		tbd		pF
<b>Switching Characteristics</b>						
Turn On Delay Time	$t_{d(on)}$	Tj = 25 °C, VDS = 800 V, ID = 5 A, Two-Level Gate Drive, RG = tbd, CG = tbd, VGH = tbd, VGL = tbd, VEE = tbd, IXDD614 Gate Drive IC, L = tbd, FWD = tbd, Refer to Fig. 15 for gate current waveform		tbd		ns
Rise Time	$t_r$			tbd		ns
Turn Off Delay Time	$t_{d(off)}$			tbd		ns
Fall Time	$t_f$			tbd		ns
Turn-On Energy Per Pulse	$E_{on}$			tbd		μJ
Turn-Off Energy Per Pulse	$E_{off}$			tbd		μJ
Total Switching Energy	$E_{ts}$		tbd		μJ	
Turn On Delay Time	$t_{d(on)}$	Tj = 175 °C, VDS = 800 V, ID = 5 A, Two-Level Gate Drive, RG = tbd, CG = tbd, VGH = tbd, VGL = tbd, VEE = tbd, IXDD614 Gate Drive IC, L = tbd, FWD = tbd, Refer to Fig. 15 for gate current waveform		tbd		ns
Rise Time	$t_r$			tbd		ns
Turn Off Delay Time	$t_{d(off)}$			tbd		ns
Fall Time	$t_f$			tbd		ns
Turn-On Energy Per Pulse	$E_{on}$			tbd		μJ
Turn-Off Energy Per Pulse	$E_{off}$			tbd		μJ
Total Switching Energy	$E_{ts}$		tbd		μJ	
<b>Thermal Characteristics</b>						
Thermal resistance, junction - case	$R_{th(jc)}$			1.41		°C/W

**Figures**

TBD

TBD

**Figure 1: Typical Output Characteristics at 25 °C**
**Figure 2: Typical Output Characteristics at 125 °C**

TBD

Figure 3: Typical Output Characteristics at 175 °C

TBD

Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

TBD

Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

TBD

Figure 6: Typical Blocking Characteristics

TBD

Figure 7: Capacitance Characteristics

TBD

Figure 8: Capacitance Characteristics

TBD

Figure 9: Typical Hard-switched Turn On Waveforms

TBD

Figure 10: Typical Hard-switched Turn Off Waveforms

TBD

Figure 11: Typical Turn On Energy Losses and Switching Times vs. Temperature

TBD

Figure 12: Typical Turn Off Energy Losses and Switching Times vs. Temperature

TBD

Figure 13: Typical Turn On Energy Losses vs. Drain Current

TBD

Figure 14: Typical Turn Off Energy Losses vs. Drain Current

TBD

Figure 15: Typical Gate Current Waveform

TBD

Figure 16: Typical Hard Switched Device Power Loss vs. Switching Frequency<sup>1</sup>

TBD

Figure 17: Power Derating Curve

TBD

Figure 18: Forward Bias Safe Operating Area

TBD

Figure 19: Turn-Off Safe Operating Area

TBD

Figure 20: Transient Thermal Impedance

<sup>1</sup> – Representative values based on device switching energy loss. Actual losses will depend on gate drive conditions, device load, and circuit topology.

**Commercial Gate Drivers Compatible with GA05JT12-263**

Manufacturer	Part Number	Peak Current Output	Optical Signal Isolation	Features		
				Desaturation Detection	Under Voltage Lockout	Active Miller Clamping
Avago Tech.	HCPL-316J	2.5	✓	✓	✓	–
Avago Tech.	HCPL-322J	2.5	✓	✓	✓	✓
IXYS	IXD_604	4.0	–	–	–	–
IXYS	IXD_609	9.0	–	–	–	–
IXYS	IXD_614	14.0	–	–	–	–
IXYS	IXD_630	30.0	–	–	–	–
IXYS	IRFD630	30.0	–	–	–	–
Micrel	MIC4452YN	12.0	–	–	–	–
Microsemi	LX1780QLQ	15.0	–	–	✓	–
Texas Instruments	UCC27322	9.0	–	–	–	–

This is a partial list of widely available commercial Silicon IGBT/MOSFET gate drivers which may be used to drive the GA05JT12-247. Specific product information including advanced features and pinouts should be obtained from the individual product manufacturer’s websites.

The gate of the GA05JT12-247 can be driven similar to a silicon IGBT or MOSFET in which a gate driver IC is used to supply positive gate current peaks to the device at turn-on and negative current peaks at turn-off. Unlike the IGBT or MOSFET, the GA05JT12-247 also requires a continuous gate current for the device to remain on after the initial current peak. An example gate current waveform for the GA05JT12-247 can be seen in Fig. 15.

**Single-Level SJT Gate Drive**

Producing the necessary gate current peaks and continuous currents can be done very simply using a circuit similar what is shown in Fig. 21 in which an external gate capacitor and resistor are placed in parallel connected to the gate drive output node and the SJT gate. The gate resistor is chosen to control the continuous gate current and adjusting the external capacitance will alter positive and negative current peaks. More details can be found in a series of GeneSiC Semiconductor Application Notes. (<http://www.genesicsemi.com/index.php/references/notes>)

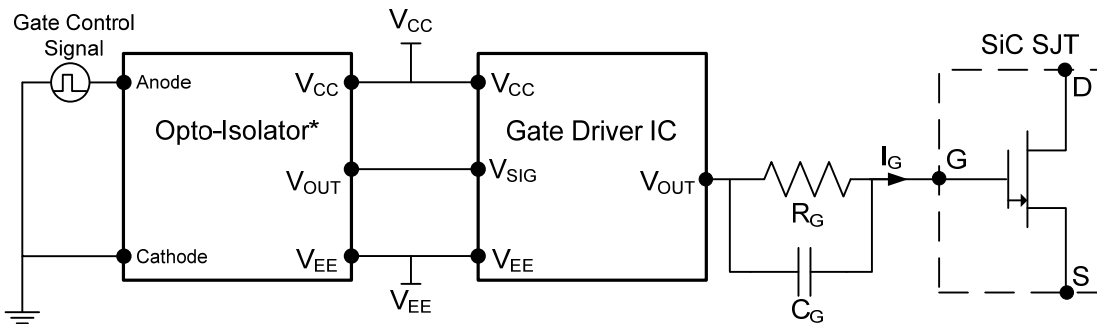


Figure 21: Single-Level SJT Gate Diver Configuration (\* – External signal isolation is required for non-isolated gate driver ICs.)

**Single-Level Gate Drive Conditions**

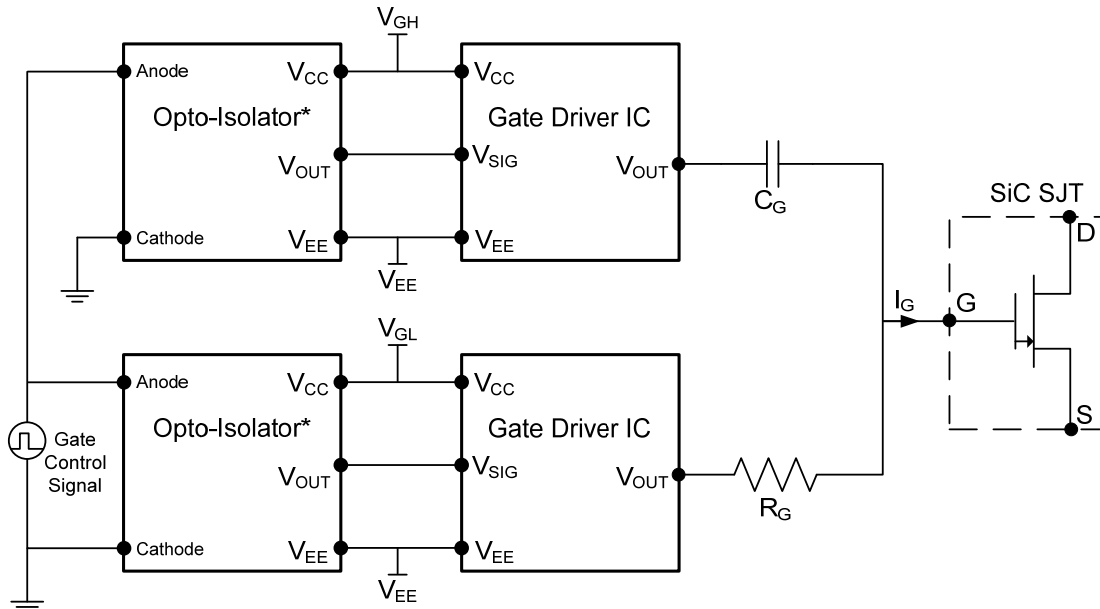
Parameter	Symbol	Conditions	Values			Unit
			Min.	Optimum	Max.	
Supply Voltage	$V_{CC}$			tbd	20	V
Negative Supply Voltage	$V_{EE}$		-10	tbd	GND	V
Output Current, Peak	$I_{OUT, pk}$	Package Limited,	1.0	tbd		A
Output Current, Continuous	$I_{OUT}$	$T = 175\text{ }^{\circ}\text{C}$	0.3	tbd		A

**Output Gate Components**

Gate Resistance	$R_G$	15	tbd		$\Omega$
Gate Capacitance	$C_G$	5	tbd		nF

**Two-Level SJT Gate Drive**

The gate of the GA05JT12-247 can also be driven with a slightly more advanced gate drive circuit, seen in Fig. 22, in which two gate drive ICs are used with two different supply voltage ( $V_{CC}$ ) levels in order to minimize gate drive losses. By using a second, lower voltage output gate driver IC the power consumption of the continuous current is reduced. Additional detail on this Two-Level SJT gate driving technique is discussed in GeneSiC Semiconductor Application Note AN-10B. (<http://www.genesicsemi.com/index.php/references/notes>)



**Figure 22: Two-Level SJT Gate Diver Configuration for Reduced Drive Losses (\* – External signal isolation is required for non-isolated gate driver ICs.)**

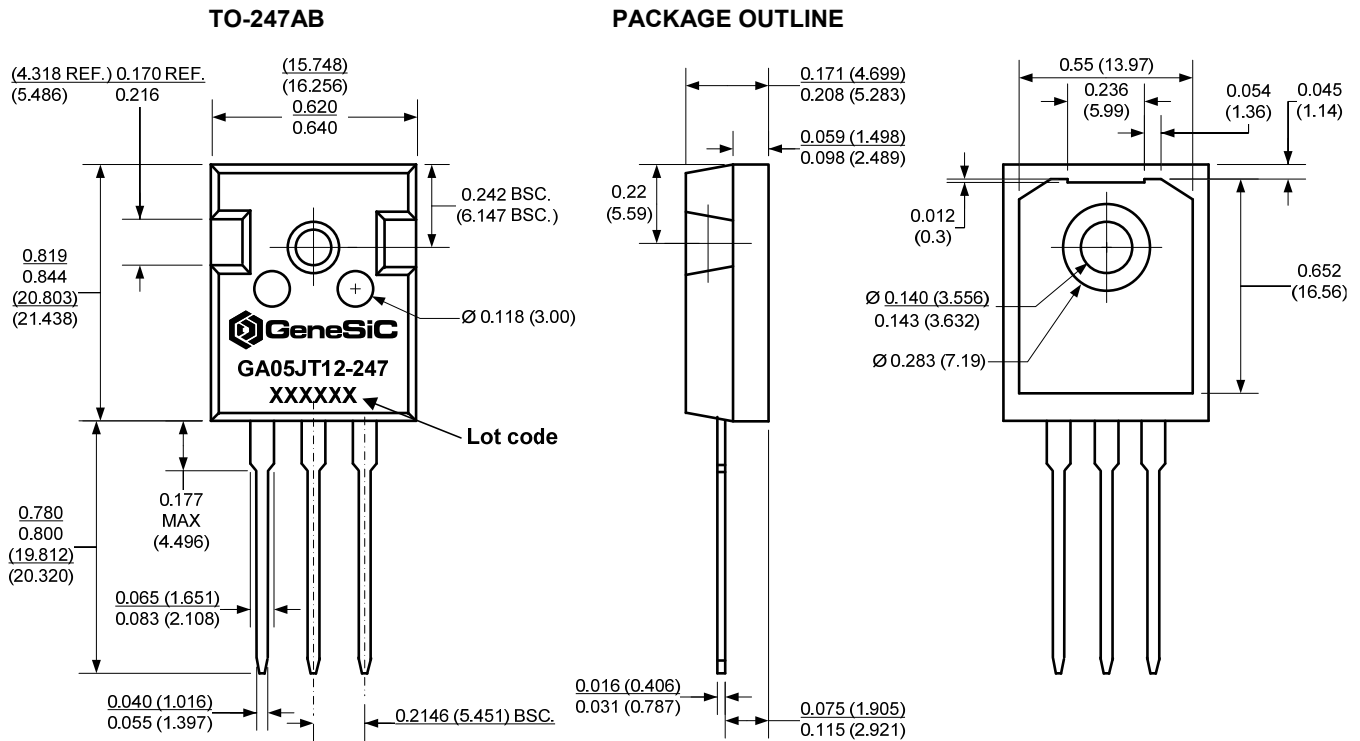
**Two-Level Gate Drive Conditions**

Parameter	Symbol	Conditions	Values			Unit
			min.	Optimum	max.	
Supply Voltage, High Level Driver	$V_{CC}(V_{GH}^+)$		15	tbd		V
Supply Voltage, Low Level Driver	$V_{CC}(V_{GL}^+)$		5	tbd		V
Negative Supply Voltage	$V_{EE}$		-10	tbd	GND	V
Output Current, Peak	$I_{OUT}$	Package Limited	1.0	tbd		A
Output Current, Continuous	$I_{OUT}$	$T = 175^\circ\text{C}$	0.3	tbd		A

**Output Gate Components**

Gate Resistance	$R_G$			tbd	5	$\Omega$
Gate Capacitance	$C_G$		5	tbd		nF

+ – Consult application note AN-10B for more information on parameters  $V_{GH}$  and  $V_{GL}$ .

**Package Dimensions:**

**NOTE**

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS

Revision History			
Date	Revision	Comments	Supersedes
2013/12/19	1	Updated Gate Drive Section	
2013/09/12	0	Initial release	

Published by  
 GeneSiC Semiconductor, Inc.  
 43670 Trade Center Place Suite 155  
 Dulles, VA 20166

GeneSiC Semiconductor, Inc. reserves right to make changes to the product specifications and data in this document without notice.

GeneSiC disclaims all and any warranty and liability arising out of use or application of any product. No license, express or implied to any intellectual property rights is granted by this document.

Unless otherwise expressly indicated, GeneSiC products are not designed, tested or authorized for use in life-saving, medical, aircraft navigation, communication, air traffic control and weapons systems, nor in applications where their failure may result in death, personal injury and/or property damage.



## SPICE Model Parameters

This is a secure document. Copy this code from the SPICE model PDF file on our website into a SPICE software program for simulation of the GA05JT12.

```
*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   1.0           $
*      $Date:      19-SEP-2013   $
*
*      GeneSiC Semiconductor Inc.
*      43670 Trade Center Place Ste. 155
*      Dulles, VA 20166
*
*      COPYRIGHT (C) 2013 GeneSiC Semiconductor Inc.
*      ALL RIGHTS RESERVED
*
*      These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
*      OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
*      TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
*      PARTICULAR PURPOSE."
*      Models accurate up to 2 times rated drain current.
*
.model GA05JT12 NPN
+ IS      5.00E-47
+ ISE     1.26E-28
+ EG      3.2
+ BF      100
+ BR      0.55
+ IKF     350
+ NF      1
+ NE      2
+ RB      0.26
+ RE      0.1
+ RC      0.115
+ CJC     1.77E-10
+ VJC     3
+ MJC     0.5
+ CJE     5.62E-10
+ VJE     3
+ MJE     0.5
+ XTI     3
+ XTB     -1.2
+ TRC1    7.00E-3
+ VCEO    1200
+ ICRATING 5
+ MFG     GeneSiC_Semiconductor
*
*      End of GA05JT12 SPICE Model
```