

RoHS Compliant Product  
 A suffix of "-C" specifies halogen & lead-free

## DESCRIPTION

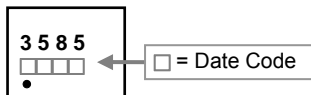
The STT3585 provide the designer with best combination of fast switching, low on-resistance and cost effectiveness.

The TSOP-6 package is universally used for all commercial-industrial surface mount applications.

## FEATURES

- Low Gate Charge
- Low On-resistance

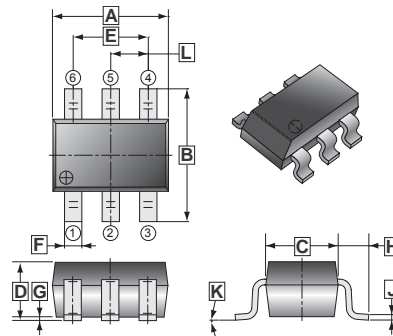
## MARKING CODE



## PACKAGE INFORMATION

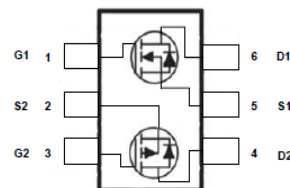
Package	MPQ	Leader Size
TSOP-6	3K	7 inch

### TSOP-6



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60	REF.
C	1.40	1.80	J	0.12	REF.
D	1.10	MAX.	K	0°	10°
E	1.90	REF.	L	0.95	REF.
F	0.30	0.50			

### TOP VIEW



## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings		Unit	
		N-Channel	P-Channel		
Drain-Source Voltage	$V_{DS}$	20	-20	V	
Gate-Source Voltage	$V_{GS}$	$\pm 12$	$\pm 12$	V	
Continuous Drain Current <sup>3</sup>	$I_D$	$T_A = 25^\circ\text{C}$	3.5	-2.5	A
		$T_A = 70^\circ\text{C}$	2.8	-1.97	
Pulsed Drain Current <sup>1</sup>	$I_{DM}$	10	-10	A	
Power Dissipation	$P_D$	1.14		W	
Maximum Junction to Ambient <sup>3</sup>	$R_{\theta JA}$	110		$^\circ\text{C} / \text{W}$	
Linear Derating Factor		0.01		$\text{W} / ^\circ\text{C}$	
Operating Junction & Storage Temperature Range	$T_J, T_{STG}$	-55~150		$^\circ\text{C}$	

**ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
<b>Static</b>							
Drain-Source Breakdown Voltage	N-Ch	BV <sub>DSS</sub>	20	-	-	V	V <sub>GS</sub> =0, I <sub>D</sub> =250μA
	P-Ch		-20	-	-		V <sub>GS</sub> =0, I <sub>D</sub> = -250μA
Breakdown Voltage Temp. Coefficient	N-Ch	ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	-	0.02	-	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
	P-Ch		-	-0.01	-		Reference to 25°C, I <sub>D</sub> = -1mA
Gate-Threshold Voltage	N-Ch	V <sub>GS(th)</sub>	0.5	-	1.2	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
	P-Ch		-	-	-1.2		V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = -250μA
Forward Transconductance	N-Ch	g <sub>fs</sub>	-	7	-	S	V <sub>DS</sub> =5V, I <sub>D</sub> =3A
	P-Ch		-	4	-		V <sub>DS</sub> = -5V, I <sub>D</sub> = -2A
Gate-Source Leakage Current	N-Ch	I <sub>GSS</sub>	-	-	±100	nA	V <sub>GS</sub> = ±12V
	P-Ch		-	-	±100		V <sub>GS</sub> = ±12V
Drain-Source Leakage Current	N-Ch	I <sub>DSS</sub>	-	-	1	μA	V <sub>DS</sub> =20 V, V <sub>GS</sub> =0
	P-Ch		-	-	-1		V <sub>DS</sub> = -20 V, V <sub>GS</sub> =0
	N-Ch		-	-	10		V <sub>DS</sub> =16V, V <sub>GS</sub> =0
	P-Ch		-	-	-25		V <sub>DS</sub> = -16V, V <sub>GS</sub> =0
Drain-Source On-Resistance <sup>1</sup>	N-Ch	R <sub>DS(ON)</sub>	-	-	75	mΩ	V <sub>GS</sub> =4.5V, I <sub>D</sub> =3.5A
	P-Ch		-	-	160		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2.5A
	N-Ch		-	-	125		V <sub>GS</sub> =2.5V, I <sub>D</sub> =1.2A
	P-Ch		-	-	300		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -2A
Total Gate Charge <sup>1</sup>	N-Ch	Q <sub>g</sub>	-	4	7	nC	N-Channel V <sub>DS</sub> =16V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =3A
	P-Ch		-	5	8		
Gate-Source Charge	N-Ch	Q <sub>gs</sub>	-	0.7	-	nC	P-Channel V <sub>DS</sub> = -16V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2A
	P-Ch		-	1	-		
Gate-Drain Charge	N-Ch	Q <sub>gd</sub>	-	2	-	nC	P-Channel V <sub>DS</sub> = -16V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2A
	P-Ch		-	2	-		
Turn-on Delay Time <sup>1</sup>	N-Ch	T <sub>d(on)</sub>	-	6	-	nS	N-Channel V <sub>DS</sub> =15V, R <sub>G</sub> =3.3Ω, R <sub>D</sub> =15Ω V <sub>GS</sub> =5V, I <sub>D</sub> =1A
	P-Ch		-	6	-		
Rise Time	N-Ch	T <sub>r</sub>	-	8	-	nS	P-Channel V <sub>DS</sub> = -10V, R <sub>G</sub> =3.3Ω, R <sub>D</sub> =10Ω V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A
	P-Ch		-	17	-		
Turn-off Delay Time	N-Ch	T <sub>d(off)</sub>	-	10	-	nS	P-Channel V <sub>DS</sub> = -10V, R <sub>G</sub> =3.3Ω, R <sub>D</sub> =10Ω V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A
	P-Ch		-	16	-		
Fall Time	N-Ch	T <sub>f</sub>	-	3	-	nS	P-Channel V <sub>DS</sub> = -10V, R <sub>G</sub> =3.3Ω, R <sub>D</sub> =10Ω V <sub>GS</sub> = -10V, I <sub>D</sub> = -1A
	P-Ch		-	5	-		
Input Capacitance	N-Ch	C <sub>iss</sub>	-	430	520	pF	N-Channel V <sub>GS</sub> =0, V <sub>DS</sub> =20V, f=1.0MHz
	P-Ch		-	630	750		
Output Capacitance	N-Ch	C <sub>oss</sub>	-	55	-	pF	P-Channel V <sub>GS</sub> =0, V <sub>DS</sub> = -20V, f=1.0MHz
	P-Ch		-	50	-		
Reverse Transfer Capacitance	N-Ch	C <sub>rss</sub>	-	40	-	pF	P-Channel V <sub>GS</sub> =0, V <sub>DS</sub> = -20V, f=1.0MHz
	P-Ch		-	40	-		
Gate Resistance	N-Ch	R <sub>g</sub>	-	1.4	1.7	Ω	f=1.0MHz
	P-Ch		-	7	10		

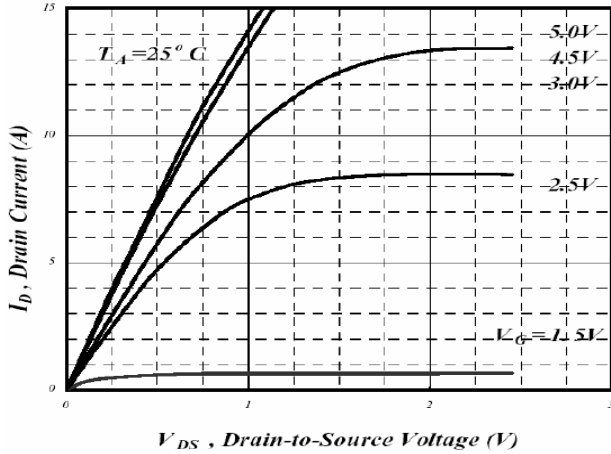
**ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
<b>Source-Drain Diode</b>							
Forward On Voltage <sup>1</sup>	N-Ch	V <sub>SD</sub>	-	-	1.2	V	I <sub>S</sub> =1.2A, V <sub>GS</sub> =0
	P-Ch		-	-	-1.2		I <sub>S</sub> = -1.2A, V <sub>GS</sub> =0
Reverse Recovery Time	N-Ch	T <sub>RR</sub>	-	16	-	ns	I <sub>S</sub> =3A, V <sub>GS</sub> =0 ,dI/dt=100A/μs
	P-Ch		-	20	-		I <sub>S</sub> = -2A, V <sub>GS</sub> =0 ,dI/dt=100A/μs
Reverse Recovery Charge	N-Ch	Q <sub>rr</sub>	-	8	-	nC	I <sub>S</sub> =3A, V <sub>GS</sub> =0 ,dI/dt=100A/μs
	P-Ch		-	15	-		I <sub>S</sub> = -2A, V <sub>GS</sub> =0 ,dI/dt=100A/μs

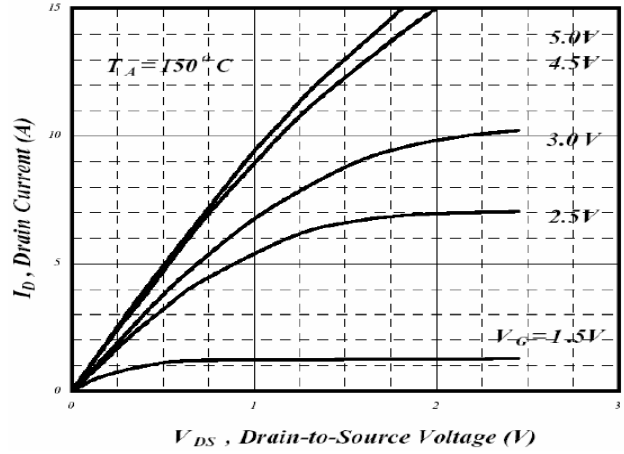
Notes:

- 1 Pulse width limited by Max. junction temperature.
- 2 Pulse width ≤ 300μs, duty cycle ≤ 2%.
- 3 Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board; t ≤ 5 sec. 180°C/W when mounted on min. copper pad.

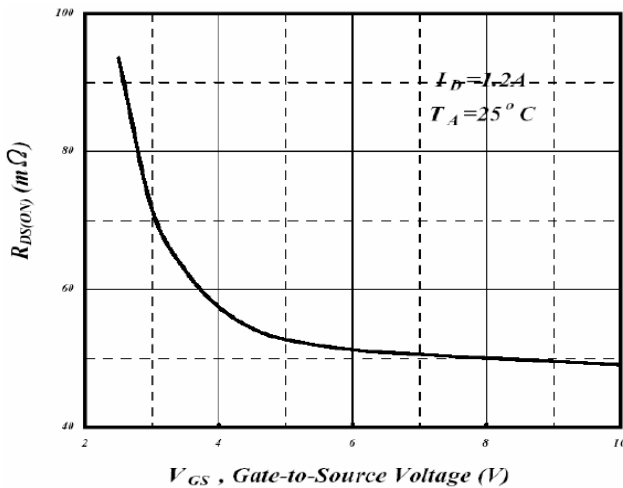
**CHARACTERISTICS CURVE (N-Channel)**



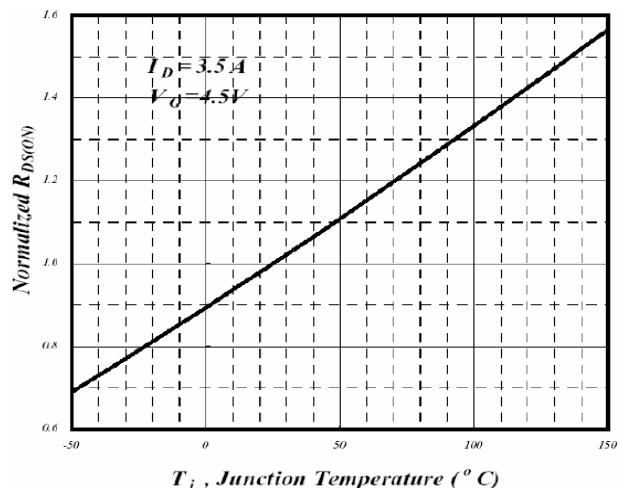
**Fig 1. Typical Output Characteristics**



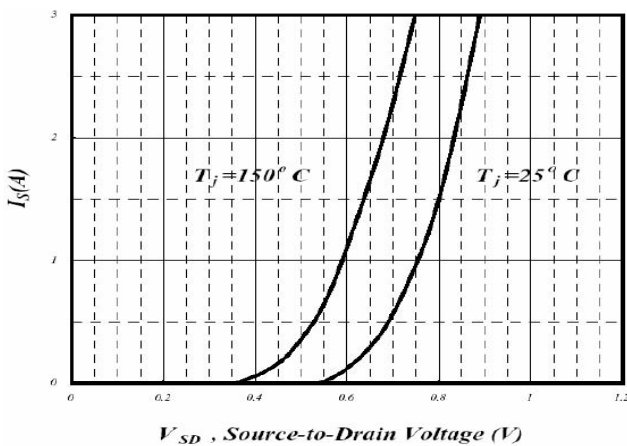
**Fig 2. Typical Output Characteristics**



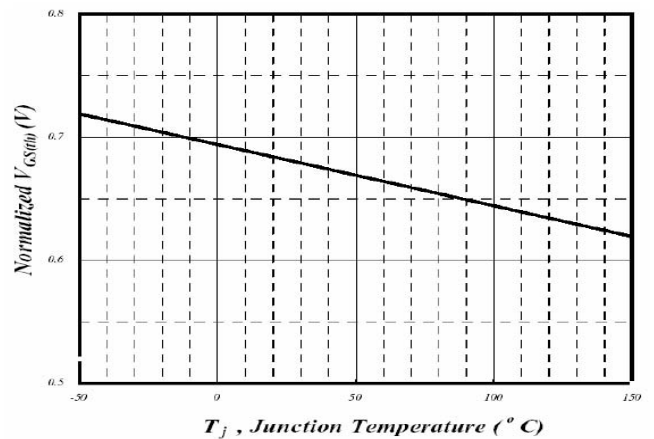
**Fig 3. On-Resistance v.s. Gate Voltage**



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

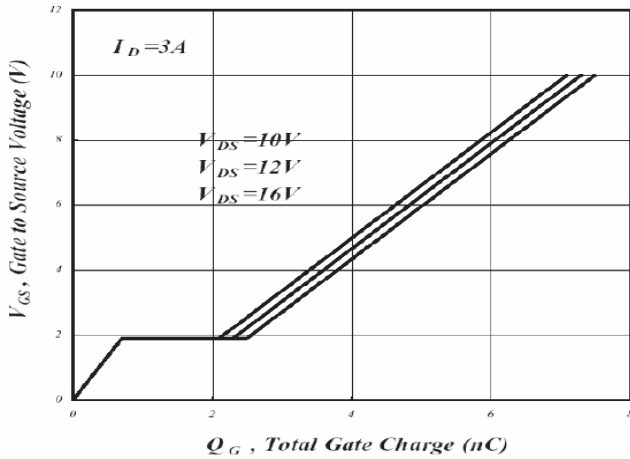


**Fig 5. Forward Characteristics of Reverse Diode**

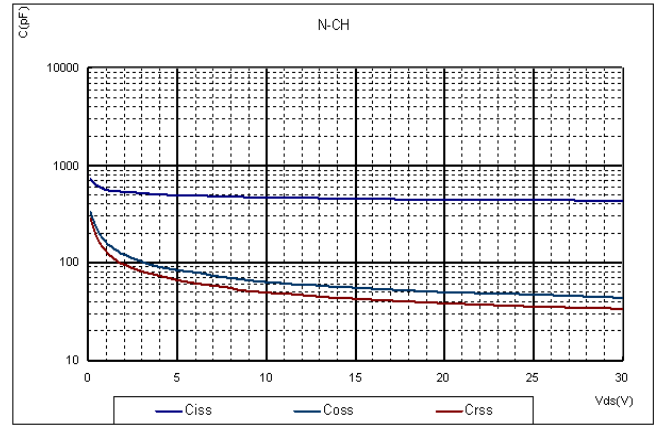


**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**

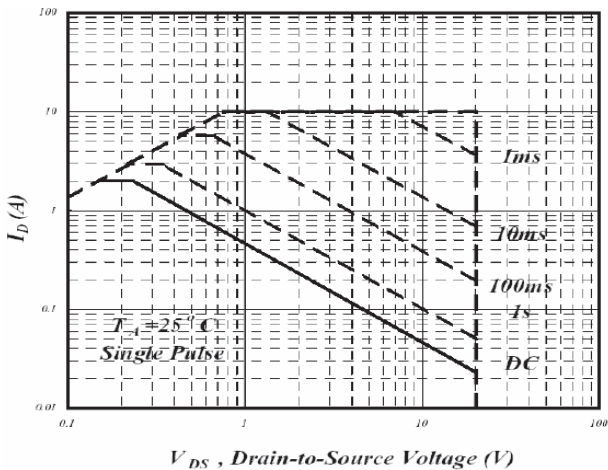
**CHARACTERISTICS CURVE (N-Channel)**



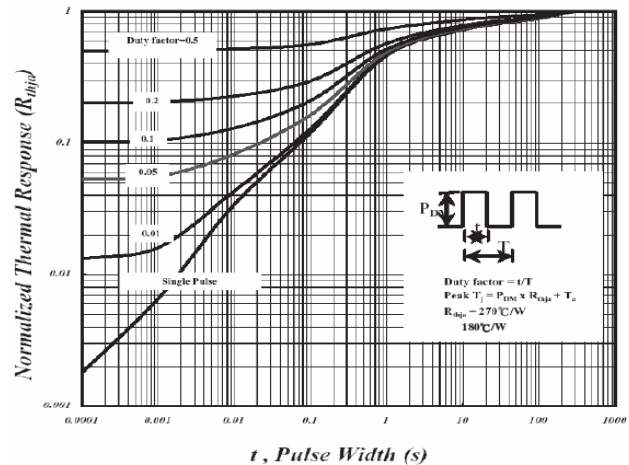
**Fig 7. Gate Charge Characteristics**



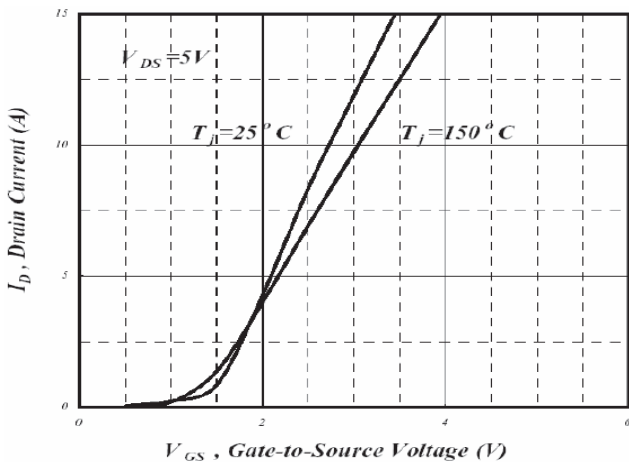
**Fig 8. Typical Capacitance Characteristics**



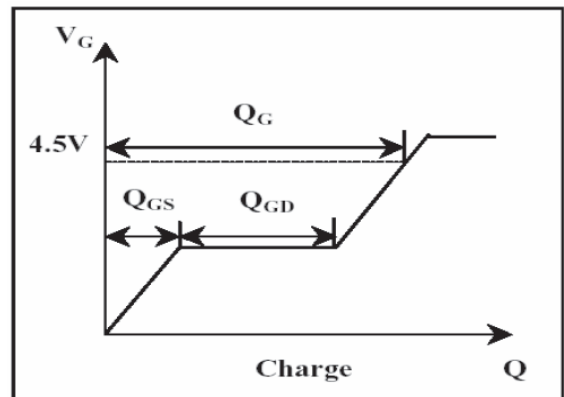
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**

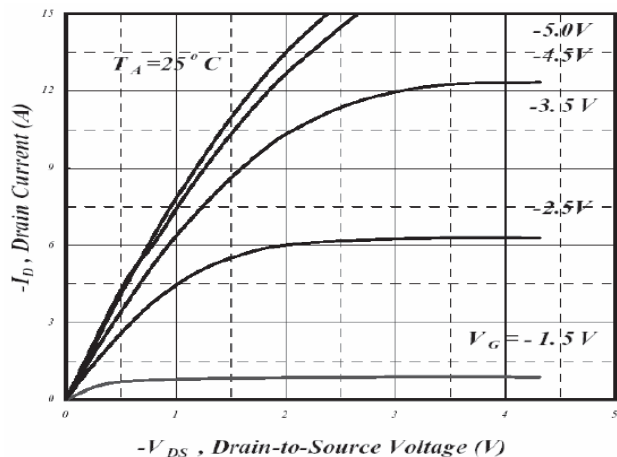


**Fig 11. Transfer Characteristics**

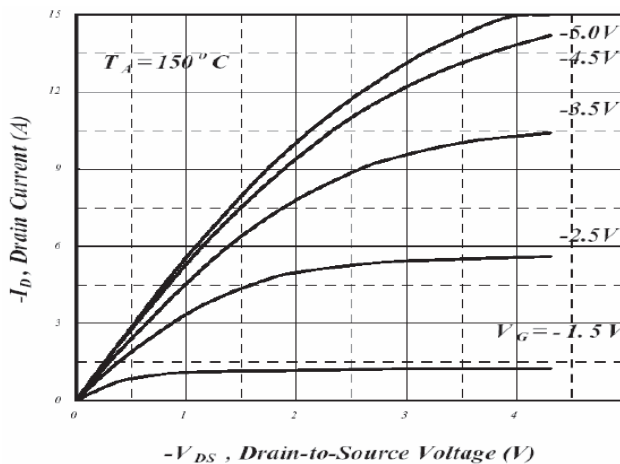


**Fig 12. Gate Charge Waveform**

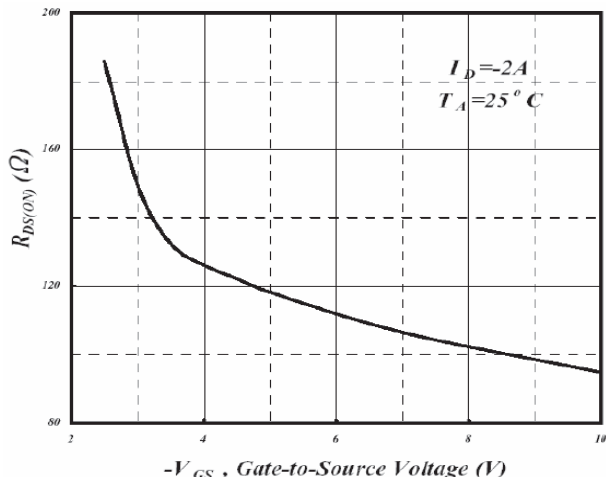
**CHARACTERISTICS CURVE (P-Channel)**



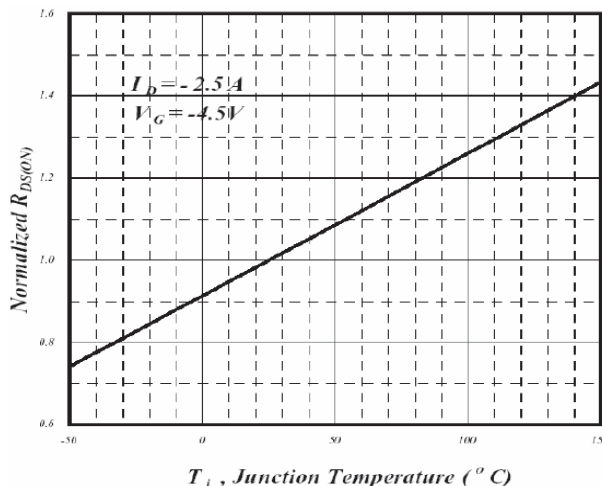
**Fig 1. Typical Output Characteristics**



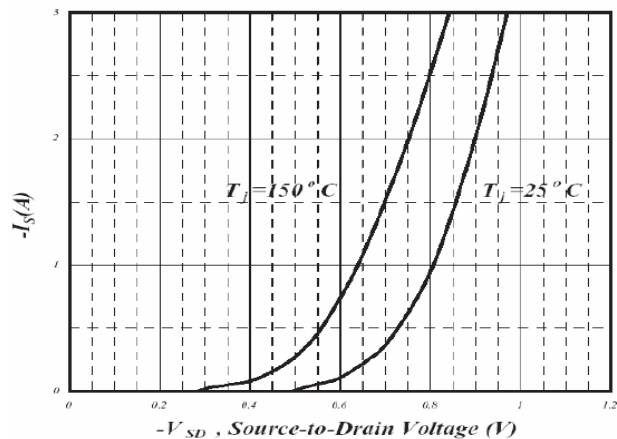
**Fig 2. Typical Output Characteristics**



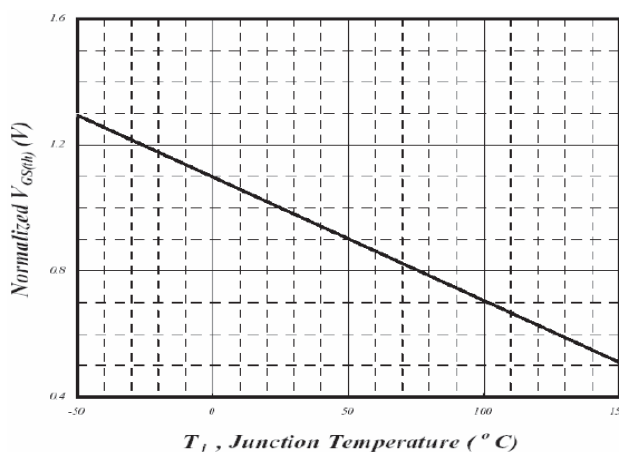
**Fig 3. On-Resistance v.s. Gate Voltage**



**Fig 4. Normalized On-Resistance v.s. Junction Temperature**

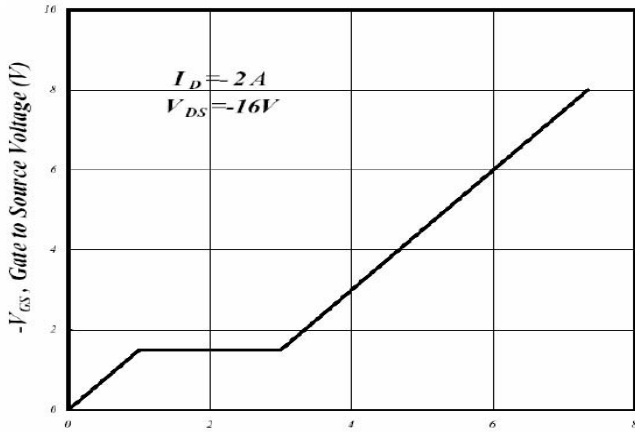


**Fig 5. Forward Characteristics of Reverse Diode**

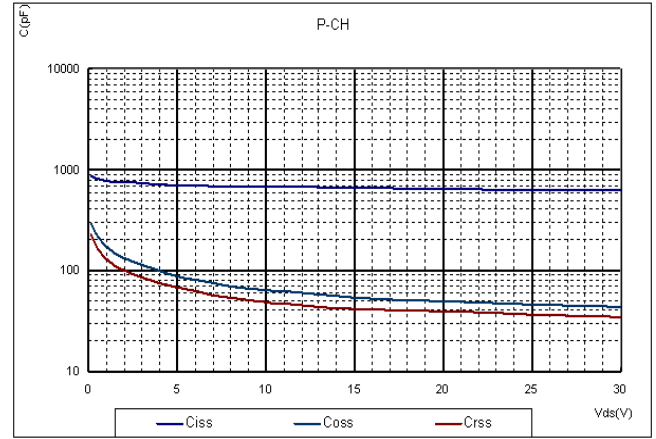


**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**

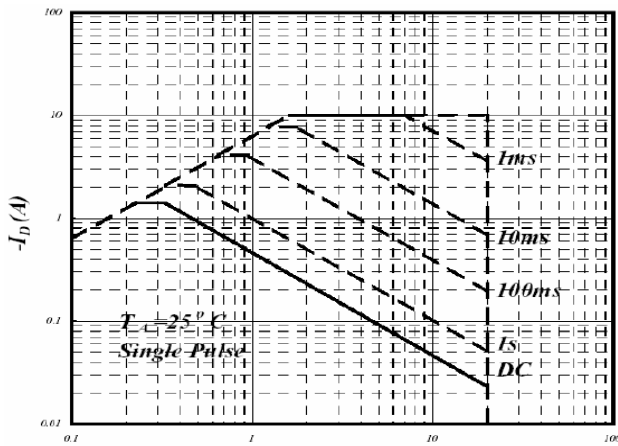
**CHARACTERISTICS CURVE (P-Channel)**



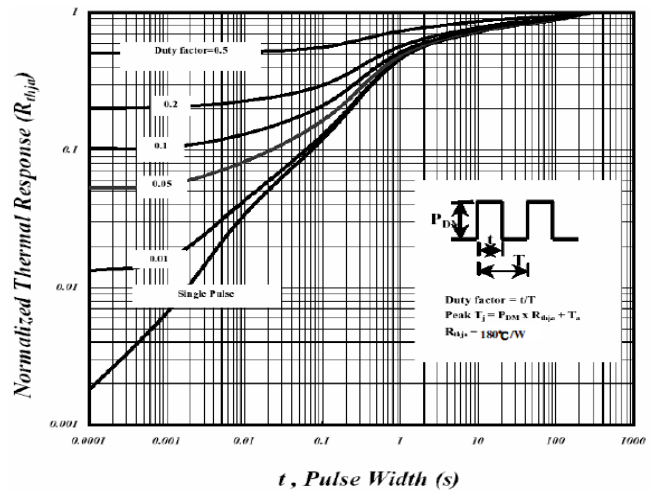
**Fig 7. Gate Charge Characteristics**



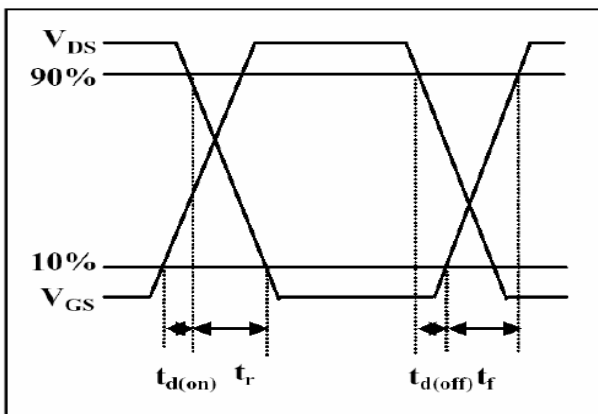
**Fig 8. Typical Capacitance Characteristics**



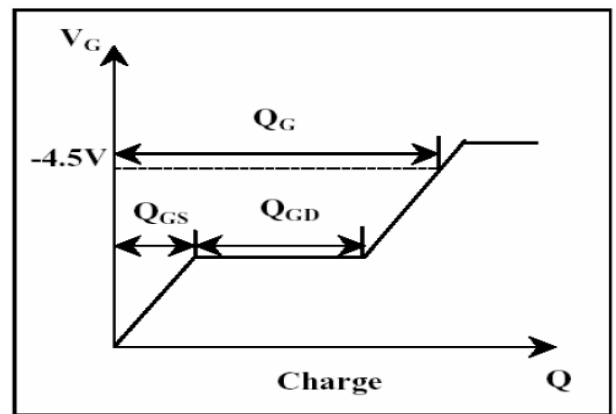
**Fig 9. Maximum Safe Operating Area**



**Fig 10. Effective Transient Thermal Impedance**



**Fig 11. Switching Time Waveform**



**Fig 12. Gate Charge Waveform**