

RoHS Compliant Product
 A suffix of "-C" specifies halogen and lead-free

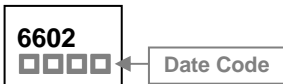
DESCRIPTION

The STT6602 uses advanced trench technology to provide excellent on-resistance and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications. The TSOP-6 package is universally used for all commercial-industrial surface mount applications.

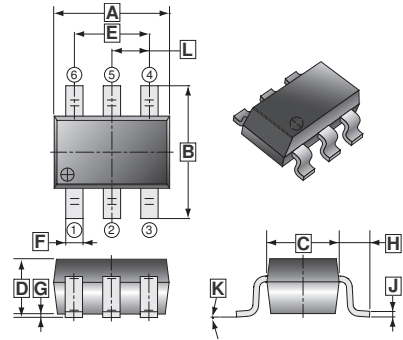
FEATURES

- Low Gate Charge
- Low On-resistance

MARKING



TSOP-6

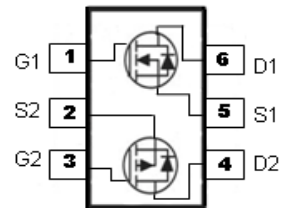


REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	0	0.10
B	2.60	3.00	H	0.60	REF.
C	1.40	1.80	J	0.12	REF.
D	1.10	MAX.	K	0°	10°
E	1.90	REF.	L	0.95	REF.
F	0.30	0.50			

PACKAGE INFORMATION

Package	MPQ	Leader Size
TSOP-6	3K	7 inch

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise specified)

Parameter	Symbol	Ratings		Unit	
		N-Channel	P-Channel		
Drain-Source Voltage	V _{DS}	30	-30	V	
Gate-Source Voltage	V _{GS}	±20	±20	V	
Continuous Drain Current ²	I _D	T _A =25°C	3.3	-2.3	A
		T _A =70°C	2.6	-1.8	
Pulsed Drain Current ¹	I _{DM}	10	-10	A	
Power Dissipation @T _A =25°C	P _D	1.14		W	
Linear Derating Factor		0.01		W / °C	
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55~150		°C	
Thermal Resistance Rating					
Maximum Junction to Ambient ²	R _{θJA}	110		°C / W	

Notes:

1. Pulse width limited by Max. junction temperature.
2. Surface mounted on 1 in² copper pad of FR4 board, t ≤ 5sec; 180°C / W when mounted on Min. copper pad.

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Static							
Drain-Source Breakdown Voltage	N-Ch	BV_{DSS}	30	-	-	V	$V_{GS}=0, I_D=250\mu\text{A}$
	P-Ch		-30	-	-		$V_{GS}=0, I_D=-250\mu\text{A}$
Gate-Threshold Voltage	N-Ch	$V_{GS(th)}$	1	-	2.5	V	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$
	P-Ch		-1	-	-2.5		$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$
Forward Transconductance	N-Ch	g_{fs}	-	4	-	S	$V_{DS}=5\text{V}, I_D=3\text{A}$
	P-Ch		-	2	-		$V_{DS}=-5\text{V}, I_D=-2\text{A}$
Gate-Source Leakage Current	N-Ch	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 20\text{V}$
	P-Ch		-	-	± 100		$V_{GS}=\pm 20\text{V}$
Drain-Source Leakage Current	N-Ch	I_{DSS}	-	-	1	uA	$V_{DS}=30\text{V}, V_{GS}=0$
	P-Ch		-	-	-1		$V_{DS}=-30\text{V}, V_{GS}=0$
	N-Ch		-	-	25		$V_{DS}=24\text{V}, V_{GS}=0$
	P-Ch		-	-	-25		$V_{DS}=-24\text{V}, V_{GS}=0$
Drain-Source On-Resistance ¹	N-Ch	$R_{DS(ON)}$	-	-	65	m Ω	$V_{GS}=10\text{V}, I_D=3\text{A}$
	P-Ch		-	-	120		$V_{GS}=-10\text{V}, I_D=-2\text{A}$
	N-Ch		-	-	90		$V_{GS}=4.5\text{V}, I_D=2\text{A}$
	P-Ch		-	-	170		$V_{GS}=-4.5\text{V}, I_D=-1\text{A}$
Total Gate Charge ¹	N-Ch	Q_g	-	3.1	-	nC	N-Channel $V_{DS}=25\text{V}, V_{GS}=4.5\text{V}, I_D=3\text{A}$
	P-Ch		-	3	-		
Gate-Source Charge	N-Ch	Q_{gs}	-	1.2	-		P-Channel $V_{DS}=-25\text{V}, V_{GS}=-4.5\text{V}, I_D=-2.0\text{A}$
	P-Ch		-	0.78	-		
Gate-Drain Charge	N-Ch	Q_{gd}	-	1.6	-		
	P-Ch		-	1.6	-		
Turn-on Delay Time ¹	N-Ch	$T_{d(on)}$	-	3.3	-	nS	N-Channel $V_{DS}=15\text{V}, R_G=3.3\Omega, R_D=15\Omega$ $V_{GS}=10\text{V}, I_D=1\text{A}$
	P-Ch		-	7	-		
Rise Time	N-Ch	T_r	-	2.5	-		P-Channel $V_{DS}=-15\text{V}, R_G=3.3\Omega, R_D=15\Omega$ $V_{GS}=-5\text{V}, I_D=-1\text{A}$
	P-Ch		-	6	-		
Turn-off Delay Time	N-Ch	$T_{d(off)}$	-	13.2	-		
	P-Ch		-	15	-		
Fall Time	N-Ch	T_f	-	1.7	-		
	P-Ch		-	7.5	-		
Input Capacitance	N-Ch	C_{iss}	-	200	-	pF	N-Channel $V_{GS}=0, V_{DS}=25\text{V}, f=1.0\text{MHz}$
	P-Ch		-	260	-		
Output Capacitance	N-Ch	C_{oss}	-	40	-		P-Channel $V_{GS}=0, V_{DS}=-25\text{V}, f=1.0\text{MHz}$
	P-Ch		-	55	-		
Reverse Transfer Capacitance	N-Ch	C_{rss}	-	20	-		
	P-Ch		-	44	-		
Gate Resistance	N-Ch	R_g	-	2.3	3.0	Ω	$f=1.0\text{MHz}$
	P-Ch		-	4.3	5		

Notes:

1. Pulse test

ELECTRICAL CHARACTERISTICS ($T_A=25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
Source-Drain Diode							
Forward On Voltage ¹	N-Ch	V_{SD}	-	-	1.2	V	$I_S=0.9\text{A}, V_{GS}=0$
	P-Ch		-	-	-1.2		$I_S=-0.9\text{A}, V_{GS}=0$
Reverse Recovery Time	N-Ch	T_{rr}	-	14	-	ns	$I_S=3\text{A}, V_{GS}=0, dI/dt=100\text{A}/\mu\text{s}$
	P-Ch		-	15	-		$I_S=-2\text{A}, V_{GS}=0, dI/dt=100\text{A}/\mu\text{s}$
Reverse Recovery Charge	N-Ch	Q_{rr}	-	7	-	nC	$I_S=3\text{A}, V_{GS}=0, dI/dt=100\text{A}/\mu\text{s}$
	P-Ch		-	7	-		$I_S=-2\text{A}, V_{GS}=0, dI/dt=100\text{A}/\mu\text{s}$

Notes:

1. Pulse test

CHARACTERISTIC CURVES (N-Channel)

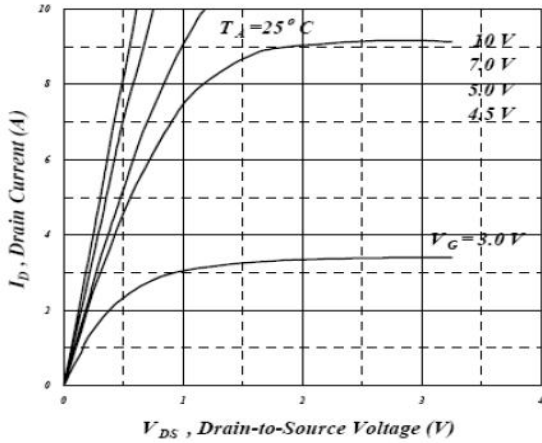


Fig 1. Typical Output Characteristics

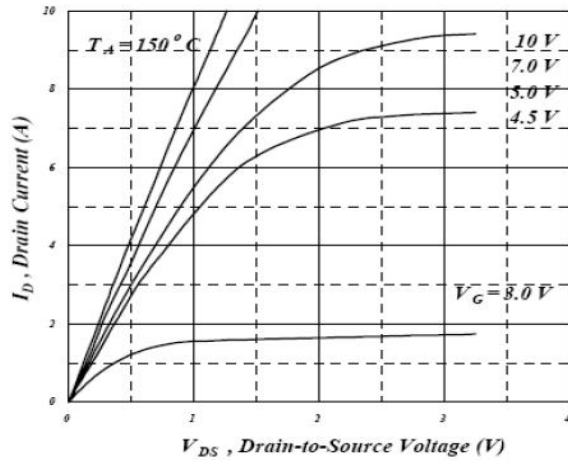


Fig 2. Typical Output Characteristics

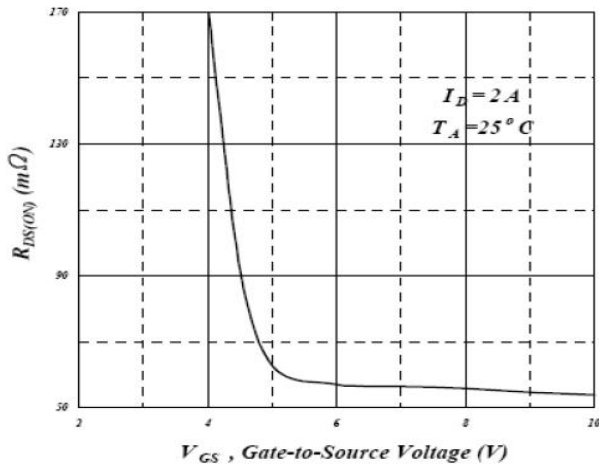


Fig 3. On-Resistance v.s. Gate Voltage

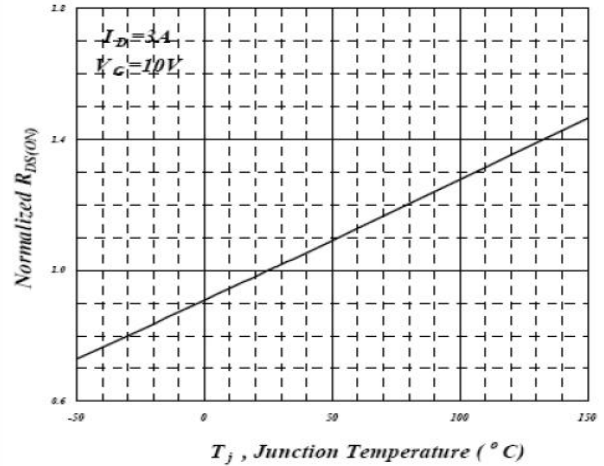


Fig 4. Normalized On-Resistance v.s. Junction Temperature

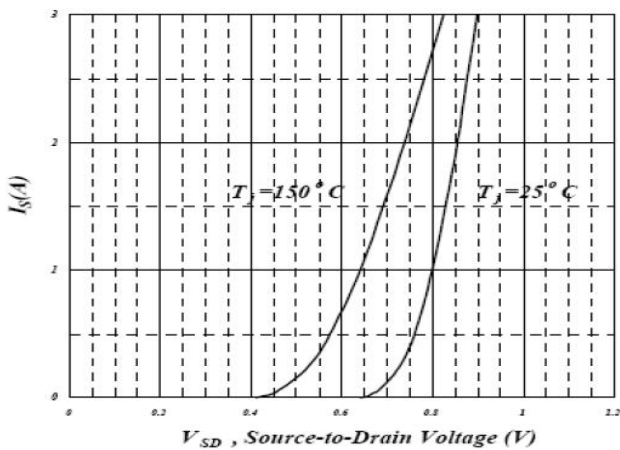


Fig 5. Forward Characteristic of Reverse Diode

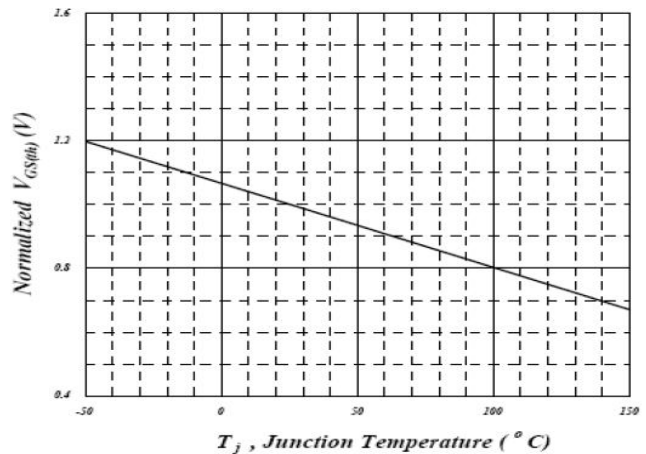


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CHARACTERISTIC CURVES (N-Channel)

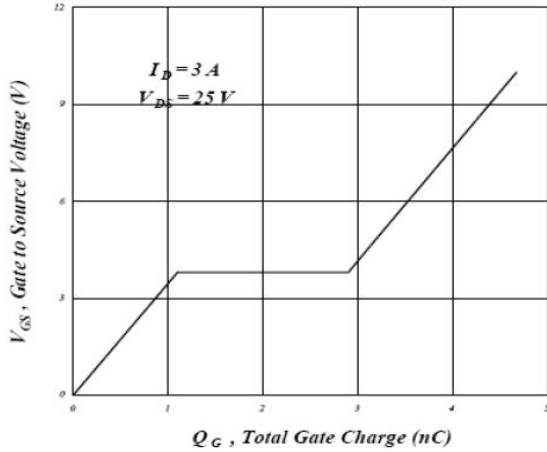


Fig 7. Gate Charge Characteristics

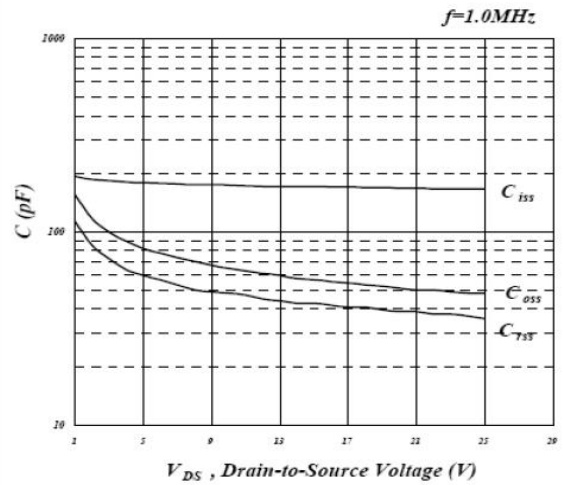


Fig 8. Typical Capacitance Characteristics

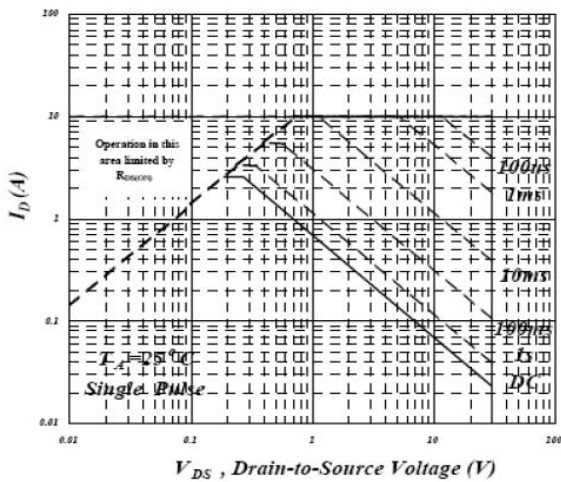


Fig 9. Maximum Safe Operating Area

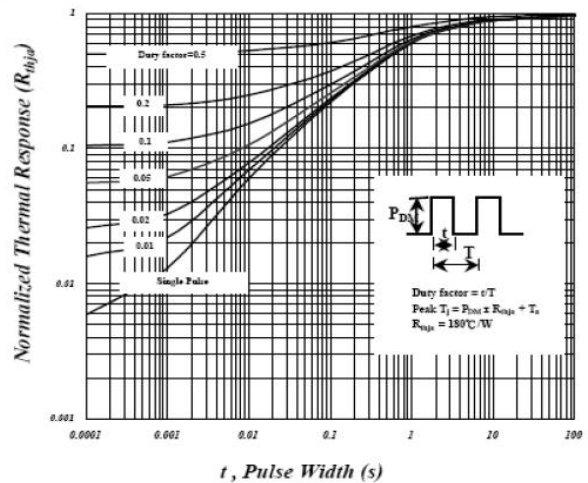


Fig 10. Effective Transient Thermal Impedance

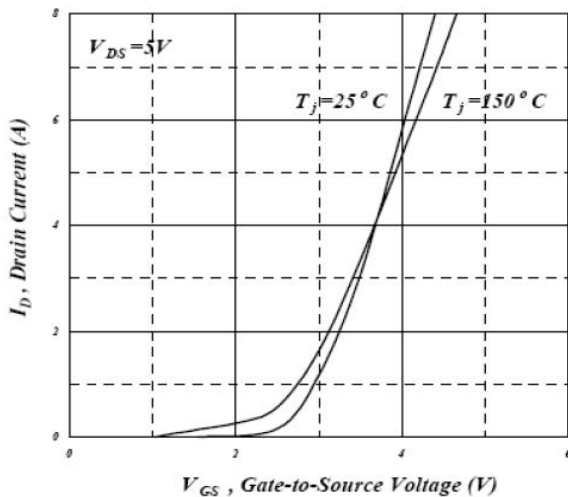


Fig 11. Transfer Characteristics

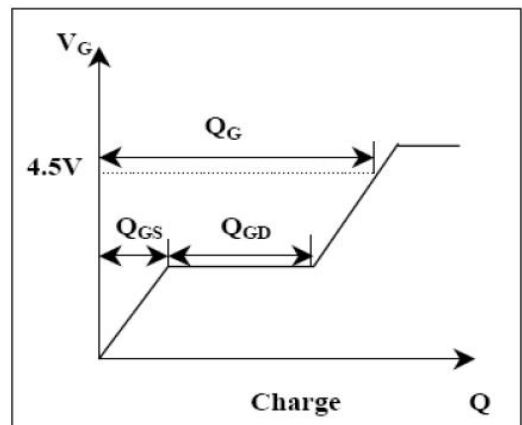


Fig 12. Gate Charge Waveform

CHARACTERISTIC CURVES (P-Channel)

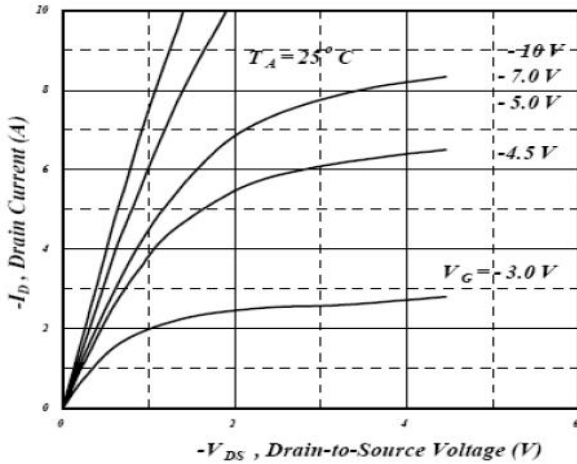


Fig 1. Typical Output Characteristics

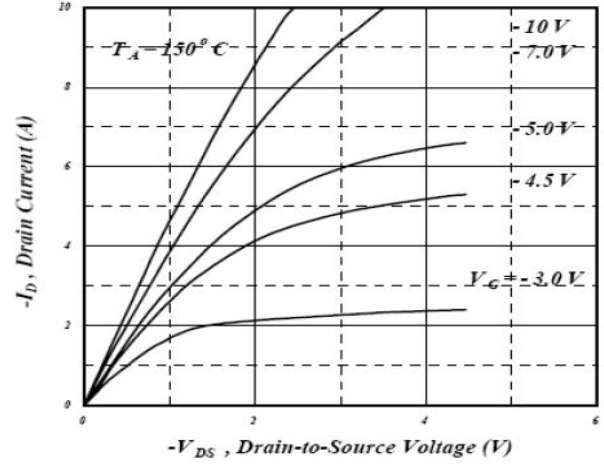


Fig 2. Typical Output Characteristics

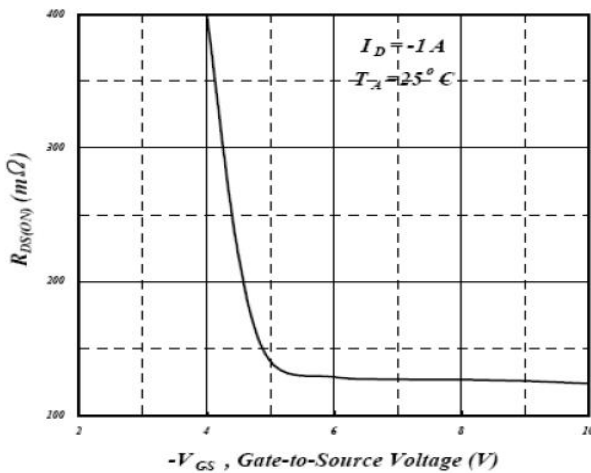


Fig 3. On-Resistance v.s. Gate Voltage

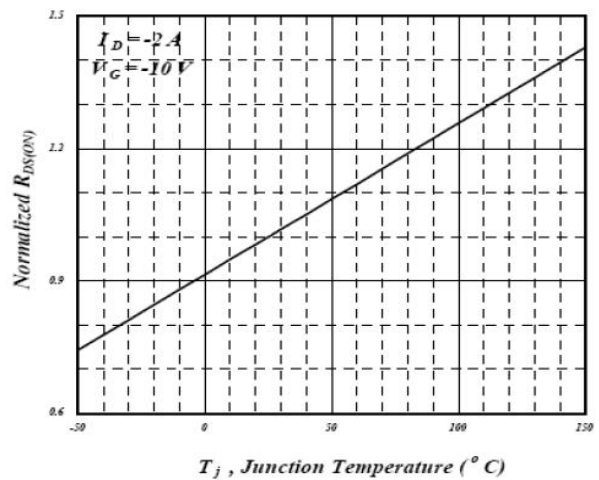


Fig 4. Normalized On-Resistance v.s. Junction Temperature

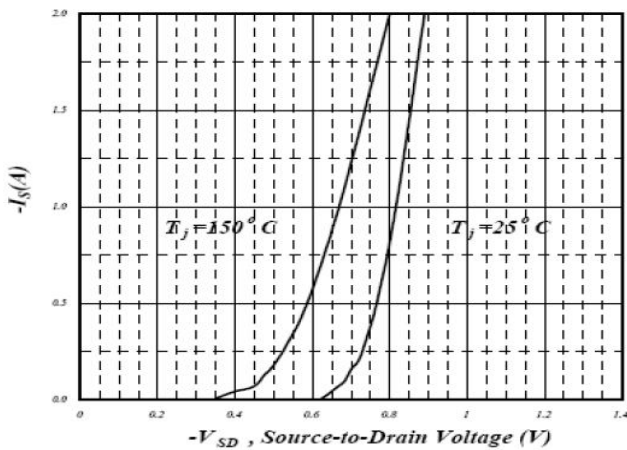


Fig 5. Forward Characteristic of Reverse Diode

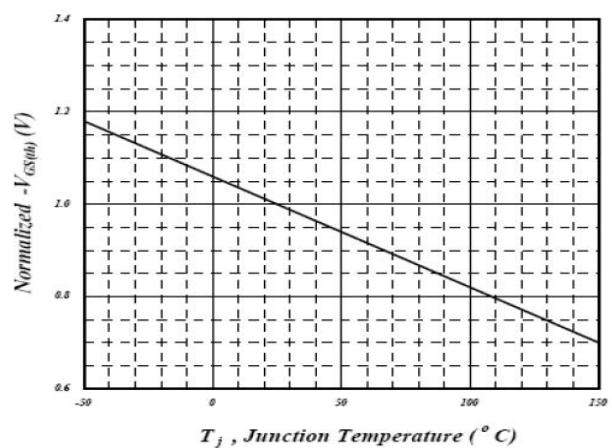


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

CHARACTERISTIC CURVES (P-Channel)

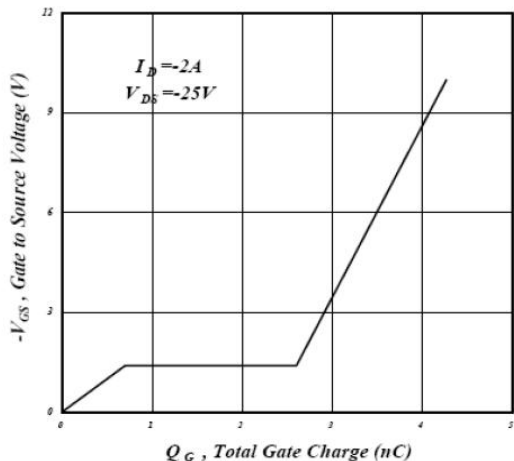


Fig 7. Gate Charge Characteristics

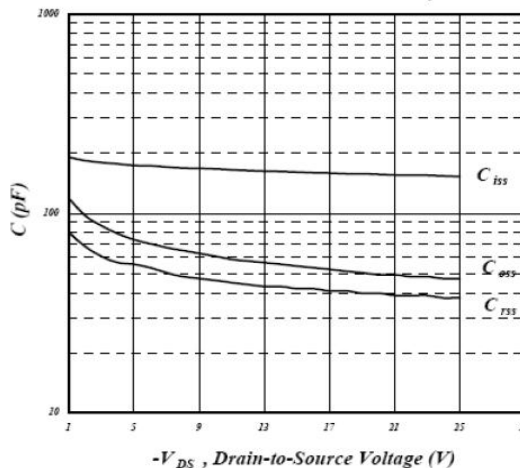


Fig 8. Typical Capacitance Characteristics

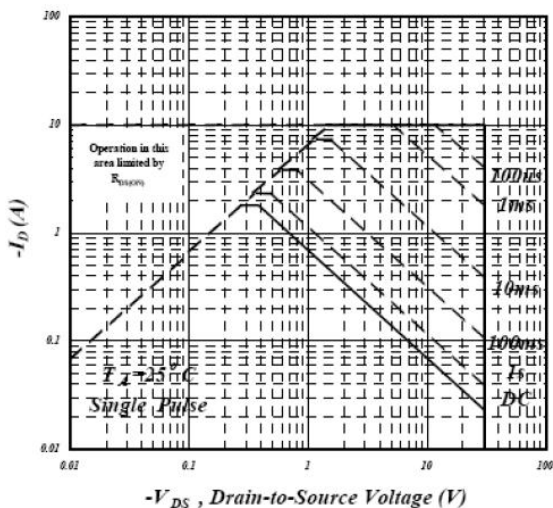


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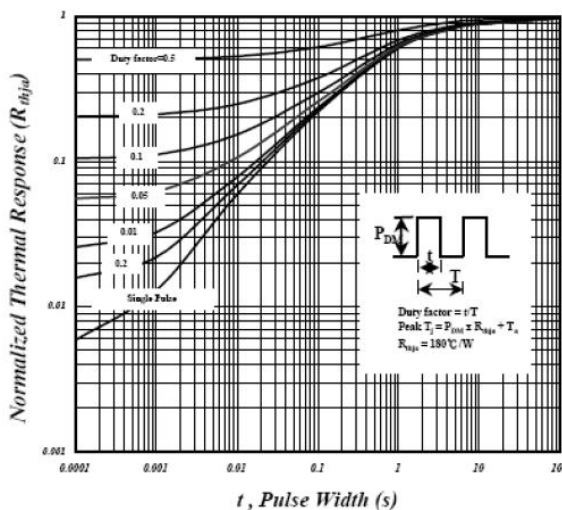


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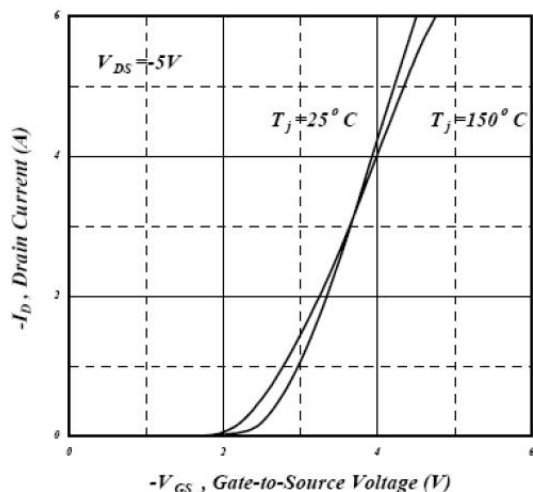


Fig 11. Transfer Characteristics

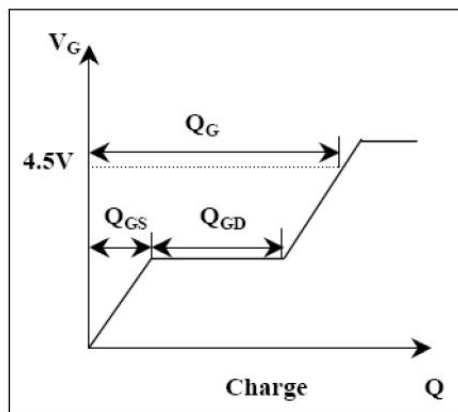


Fig 12. Gate Charge Waveform