

## 16V P-Channel Enhancement-Mode MOSFET

$V_{DS} = -16V$

$R_{DS(ON)}, V_{GS} @ -4.5V, I_{DS} @ -4.7A = 60\ m\Omega$

$R_{DS(ON)}, V_{GS} @ -2.5V, I_{DS} @ -1.0A = 100\ m\Omega$

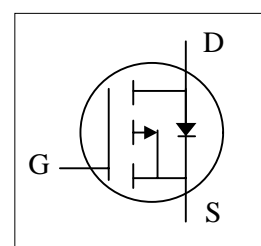
### Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

- ▼ Simple Drive Requirement
- ▼ Small Package Outline
- ▼ Surface Mount Device

LP2307LT1G



### ORDERING INFORMATION

Device	Marking	Shipping
LP2307LT1G	P07	3000/Tape&Reel
LP2307LT3G	P07	10000/Tape&Reel

### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-16	V
$V_{GS}$	Gate-Source Voltage	$\pm 8$	V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current <sup>3</sup>	-4.7	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current <sup>3</sup>	-3.3	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	-20	A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	1.1	W
$P_D @ T_A = 70^\circ C$	Total Power Dissipation	0.7	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

### Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient <sup>3</sup>	110	$^\circ C/W$

## LP2307LT1G

**Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-16	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=-4.5V, I_D=-4.7A$	-	48	60	$m\Omega$
		$V_{GS}=-2.7V, I_D=-3.8A$	-	63	90	$m\Omega$
		$V_{GS}=-2.5V, I_D=-1.0A$	-	65	100	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.6	-0.85	-1.4	V
$g_{fs}$	Forward Transconductance	$V_{DS}=-10V, I_D=-4.7A$	-	8	-	S
$I_{DSS}$	Drain-Source Leakage Current ( $T_j=25^{\circ}\text{C}$ )	$V_{DS}=-16V, V_{GS}=0V$	-	-	-1	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 8V, V_{DS}=0V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=-4.7A$	-	24	36	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=-10V$	-	18	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=-4.5V$	-	2.7	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=-10V$	-	22	35	ns
$t_r$	Rise Time	$I_D=-1A$	-	35	55	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=6\Omega, V_{GS}=-4.5V$	-	45	70	ns
$t_f$	Fall Time	$R_D=10\Omega$	-	25	40	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	985	1580	pF
$C_{oss}$	Output Capacitance	$V_{DS}=-15V$	-	180	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	160	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$I_S$	Max Diode Forward Current				-1.7	A
$V_{SD}$	Diode Forward Voltage	$I_S=-1.7A, V_{GS}=0V$			-1.2	V

**Notes:**

1. Pulse width limited by Max. junction temperature.
2. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board; 270°C/W when mounted on min. copper pad.

# LP2307LT1G

## TYPICAL ELECTRICAL CHARACTERISTICS

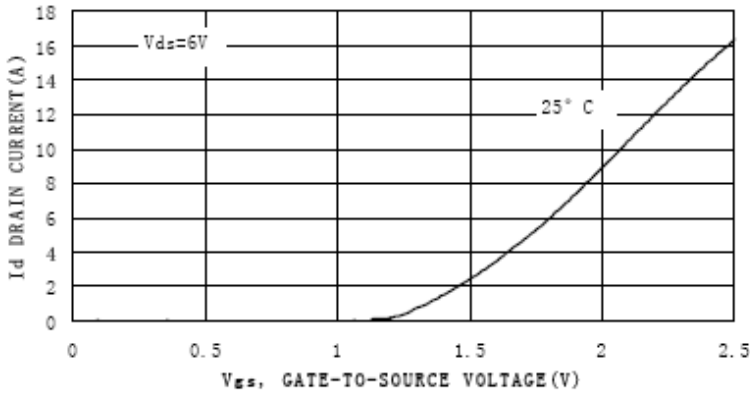


Figure 1. Transfer Characteristics

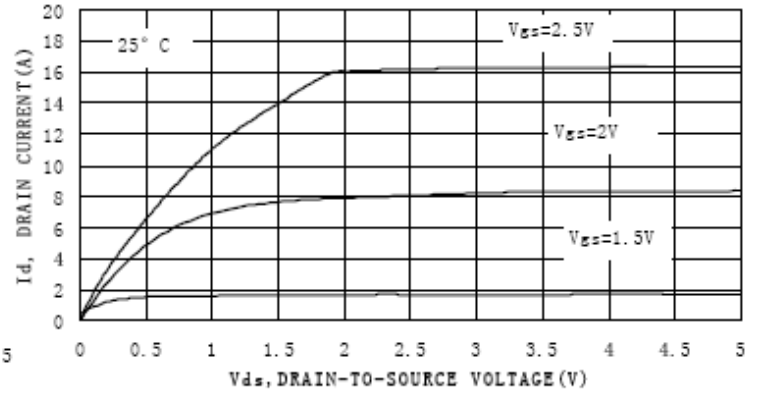


Figure 2. On-Region Characteristics

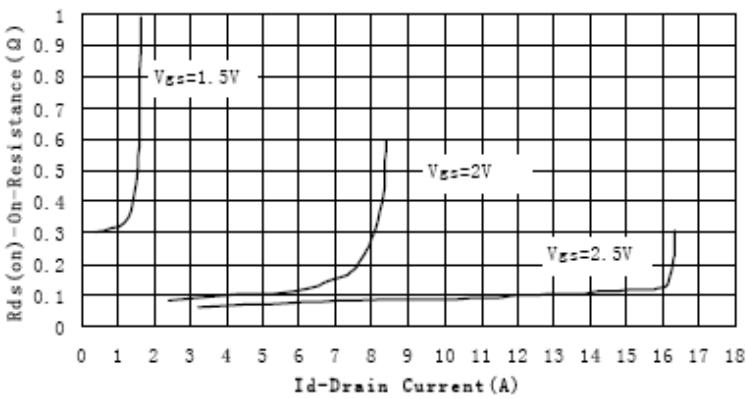


Figure 3. On-Resistance versus Drain Current

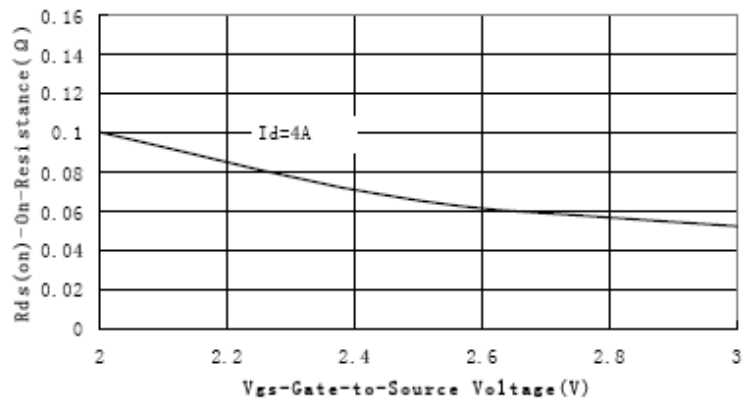


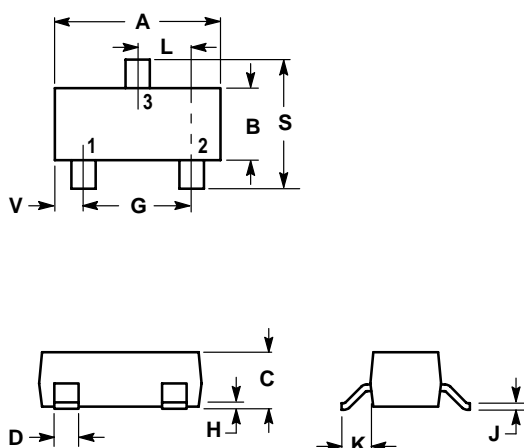
Figure 4. On-Resistance vs. Gate-to-Source Voltage

LP2307LT1G

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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60

