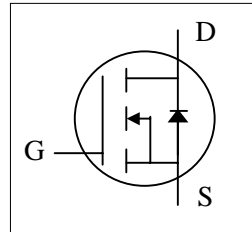
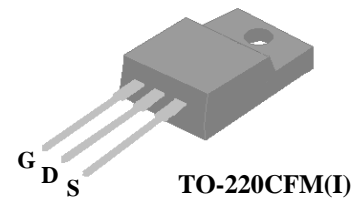




- ▼ Fast trr Performance
- ▼ Fast Switching Characteristic
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	500V
$R_{DS(ON)}$	1.8 Ω
I_D	4.4A



Description

AP05FN50 series are specially designed as main switching devices for universal 90~265VAC off-line AC/DC converter applications. It provide high blocking voltage to overcome voltage surge and sag in the toughest power system with the best combination of fast switching design and cost-effectiveness.

The TO-220CFM package is widely preferred for all commercial-industrial through hole applications. The mold compound provides a high isolation voltage capability and low thermal resistance between the tab and the external heat-sink.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	4.4	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.7	A
I_{DM}	Pulsed Drain Current ¹	18	A
$P_D @ T_C = 25^\circ C$	Total Power Dissipation	31.3	W
$P_D @ T_A = 25^\circ C$	Total Power Dissipation	1.92	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	4	$^\circ C/W$
Rthj-a	Maximum Thermal Resistance, Junction-ambient	65	$^\circ C/W$



Electrical Characteristics @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	500	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =2.7A	-	-	1.8	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =2.7A	-	4.5	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =500V, V _{GS} =0V	-	-	25	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =1A	-	20	32	nC
Q _{gs}	Gate-Source Charge	V _{DS} =400V	-	3.3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	6.5	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DD} =250V	-	9	-	ns
t _r	Rise Time	I _D =3.1A	-	8	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =12Ω	-	36	-	ns
t _f	Fall Time	V _{GS} =10V	-	13.5	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	900	1440	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	90	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	5	-	pF
R _g	Gate Resistance	f=1.0MHz	-	2.5	5	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =4.5A, V _{GS} =0V	-	-	1.5	V
t _{rr}	Reverse Recovery Time	I _S =3.1A, V _{GS} =0V,	-	75	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	185	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

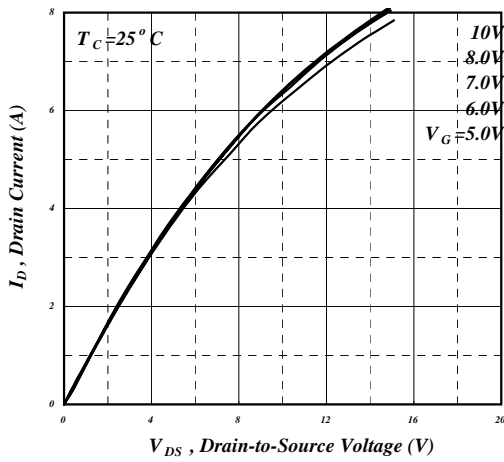


Fig 1. Typical Output Characteristics

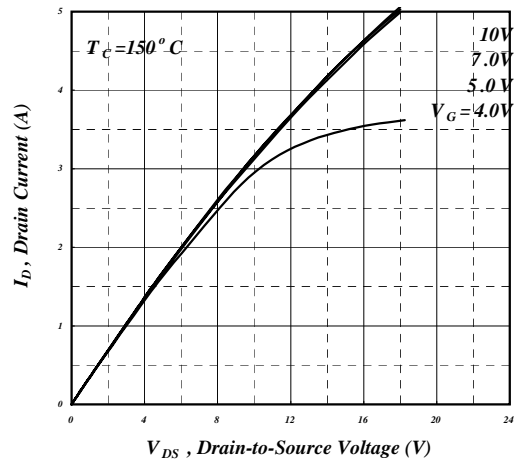


Fig 2. Typical Output Characteristics

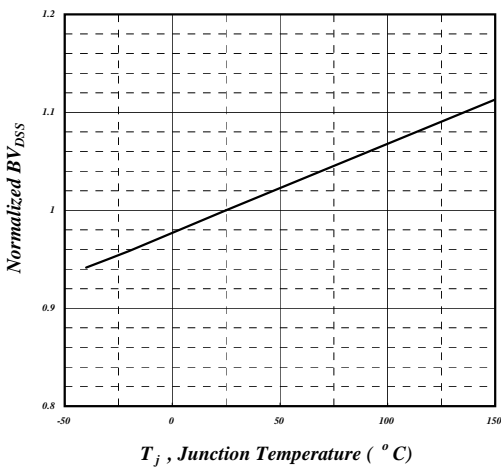


Fig 3. Normalized BV_{DSS} v.s. Junction Temperature

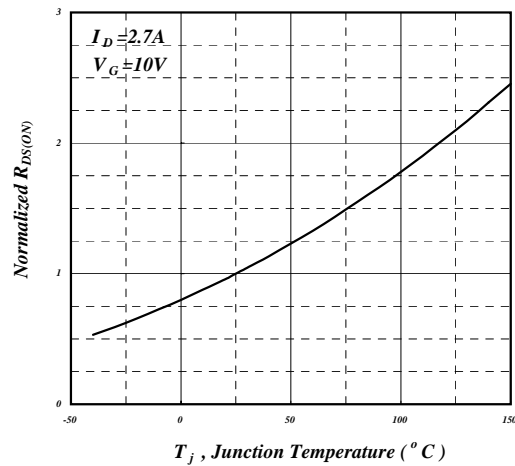


Fig 4. Normalized On-Resistance v.s. Junction Temperature

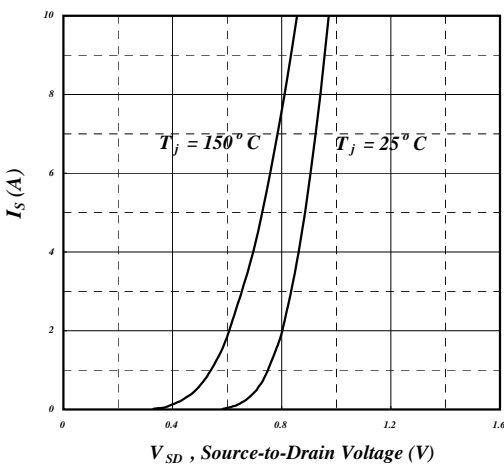


Fig 5. Forward Characteristic of Reverse Diode

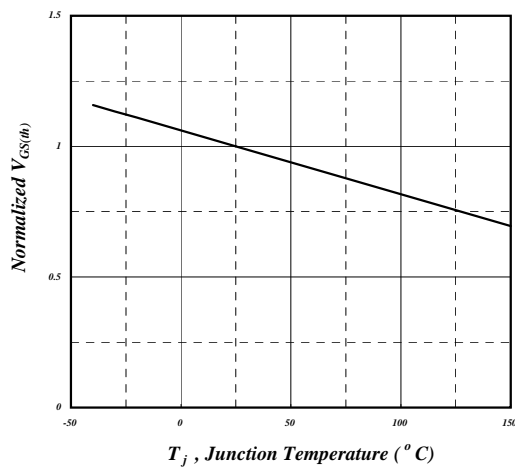


Fig 6. Gate Threshold Voltage v.s. Junction Temperature



AP05FN50I-HF

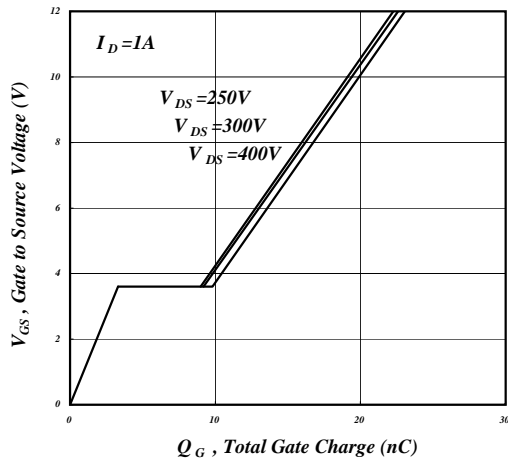


Fig 7. Gate Charge Characteristics

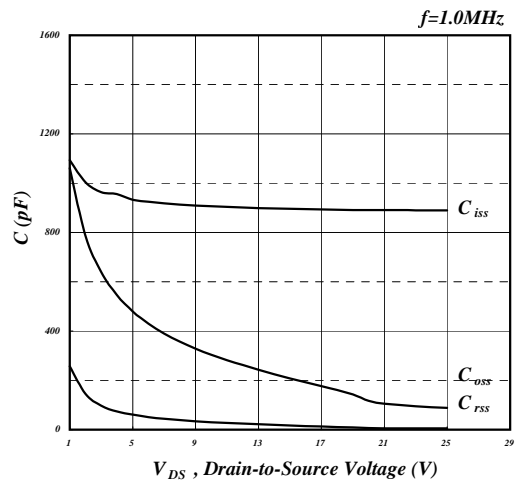


Fig 8. Typical Capacitance Characteristics

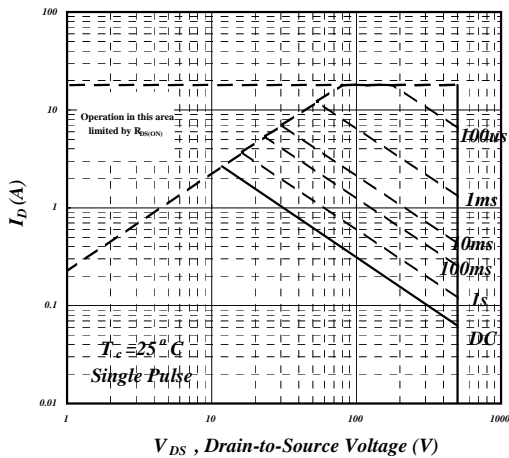


Fig 9. Maximum Safe Operating Area

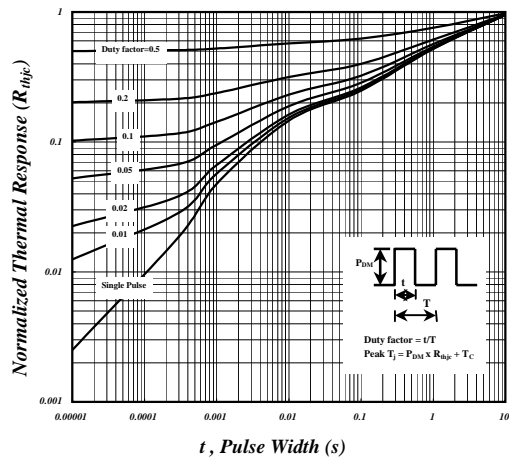


Fig 10. Effective Transient Thermal Impedance



Fig 11. Switching Time Waveform

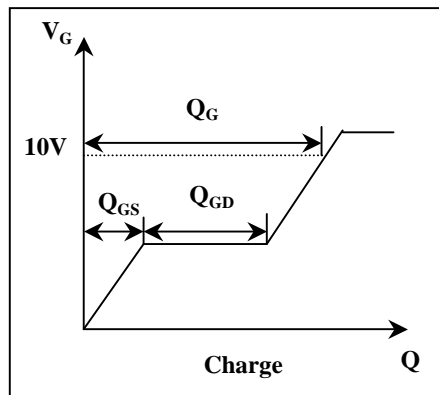


Fig 12. Gate Charge Waveform