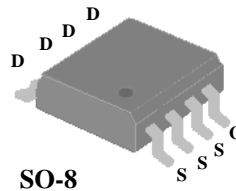




- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ Fast Switching Characteristic
- ▼ RoHS Compliant

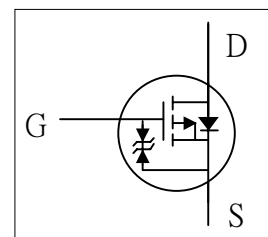


| | |
|--------------|---------------|
| BV_{DSS} | -35V |
| $R_{DS(ON)}$ | 7.5m Ω |
| I_D | -14.5A |

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|----------------------|--|------------|---------------|
| V_{DS} | Drain-Source Voltage | -35 | V |
| V_{GS} | Gate-Source Voltage | ± 20 | V |
| $I_D@T_A=25^\circ C$ | Continuous Drain Current ^{3a} | -14.5 | A |
| $I_D@T_A=70^\circ C$ | Continuous Drain Current ^{3a} | -12 | A |
| I_{DM} | Pulsed Drain Current ¹ | -50 | A |
| $P_D@T_A=25^\circ C$ | Total Power Dissipation | 2.5 | W |
| | Linear Derating Factor | 0.02 | W/ $^\circ C$ |
| T_{STG} | Storage Temperature Range | -55 to 150 | $^\circ C$ |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ C$ |

Thermal Data

| Symbol | Parameter | Value | Unit |
|--------|--|-------|--------------|
| Rthj-a | Maximum Thermal Resistance, Junction-ambient ^{3a} | 50 | $^\circ C/W$ |

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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AP4409AGEM-HF

Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

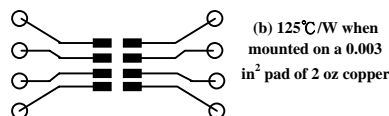
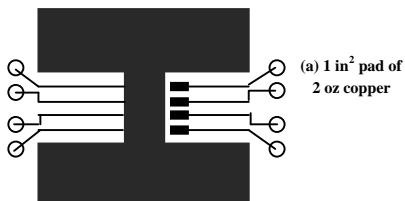
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|--------------|--|---|------|------|----------|-----------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=-250\mu A$ | -35 | - | - | V |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance ² | $V_{GS}=-10V, I_D=-7A$ | - | - | 7.5 | $m\Omega$ |
| | | $V_{GS}=-4V, I_D=-7A$ | - | - | 15 | $m\Omega$ |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}, I_D=-250\mu A$ | -1 | - | -3 | V |
| g_{fs} | Forward Transconductance | $V_{DS}=-10V, I_D=-7A$ | - | 7 | - | S |
| I_{DSS} | Drain-Source Leakage Current | $V_{DS}=-30V, V_{GS}=0V$ | - | - | -10 | μA |
| | | Drain-Source Leakage Current ($T_j=70^\circ\text{C}$) | - | - | -25 | μA |
| I_{GSS} | Gate-Source Leakage | $V_{GS}=\pm 20V$ | - | - | ± 30 | μA |
| Q_g | Total Gate Charge ² | $I_D=-14A$ | - | 58 | 90 | nC |
| Q_{gs} | Gate-Source Charge | $V_{DS}=-30V$ | - | 7 | - | nC |
| Q_{gd} | Gate-Drain ("Miller") Charge | $V_{GS}=-4.5V$ | - | 37 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time ² | $V_{DS}=-15V$ | - | 15 | - | ns |
| t_r | Rise Time | $I_D=-1A$ | - | 13 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | $R_G=3.3\Omega, V_{GS}=-10V$ | - | 76 | - | ns |
| t_f | Fall Time | $R_D=15\Omega$ | - | 60 | - | ns |
| C_{iss} | Input Capacitance | $V_{GS}=0V$ | - | 4100 | 6600 | pF |
| C_{oss} | Output Capacitance | $V_{DS}=-25V$ | - | 640 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | $f=1.0\text{MHz}$ | - | 530 | - | pF |

Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|----------|------------------------------------|------------------------|------|------|------|-------|
| V_{SD} | Forward On Voltage ² | $I_S=-14A, V_{GS}=0V$ | - | - | -1.3 | V |
| t_{rr} | Reverse Recovery Time ² | $I_S=-14A, V_{GS}=0V,$ | - | 46 | - | ns |
| Q_{rr} | Reverse Recovery Charge | $dI/dt=100A/\mu s$ | - | 44 | - | nC |

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board (a), $t \leq 10\text{sec}$



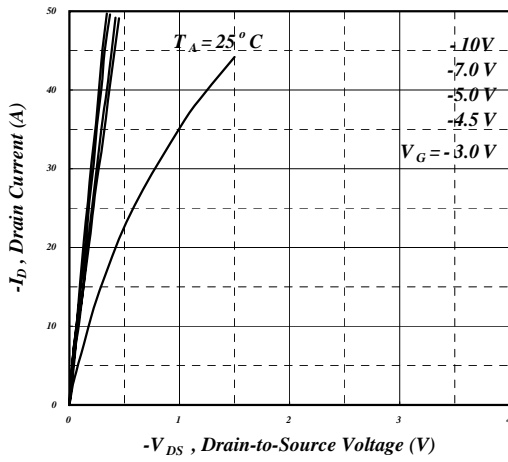


Fig 1. Typical Output Characteristics

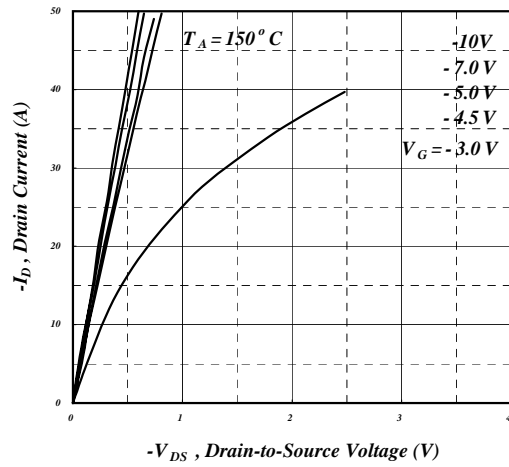


Fig 2. Typical Output Characteristics

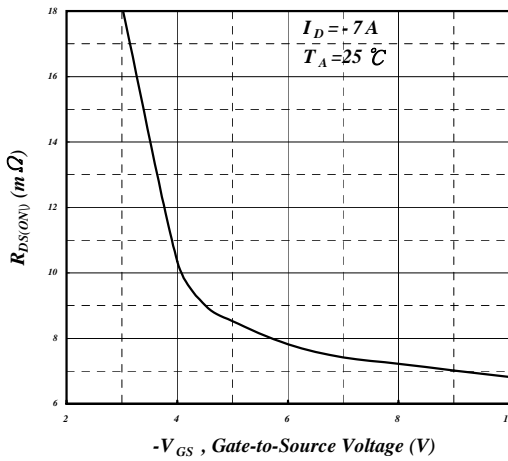


Fig 3. On-Resistance v.s. Gate Voltage

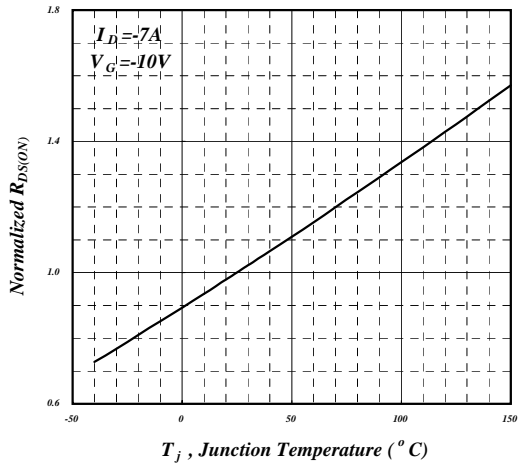


Fig 4. Normalized On-Resistance v.s. Junction Temperature

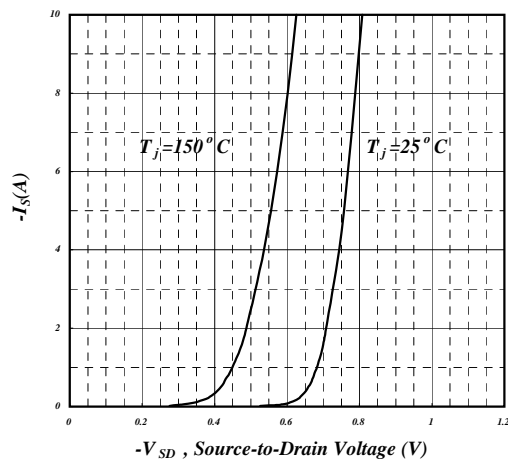


Fig 5. Forward Characteristic of Reverse Diode

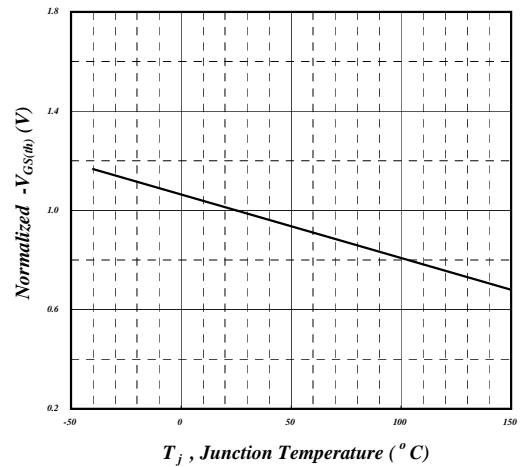


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

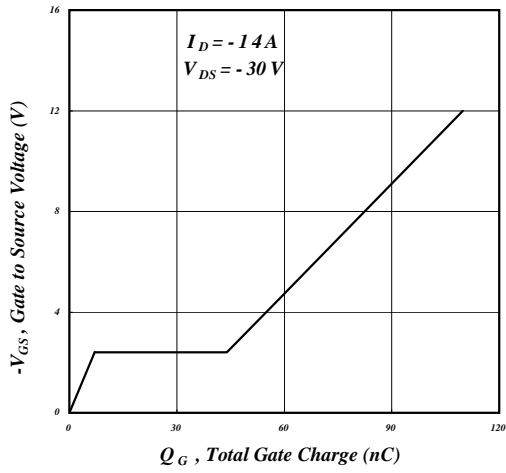


Fig 7. Gate Charge Characteristics

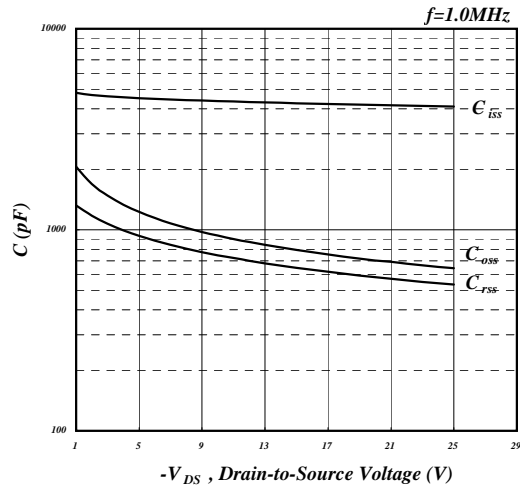


Fig 8. Typical Capacitance Characteristics

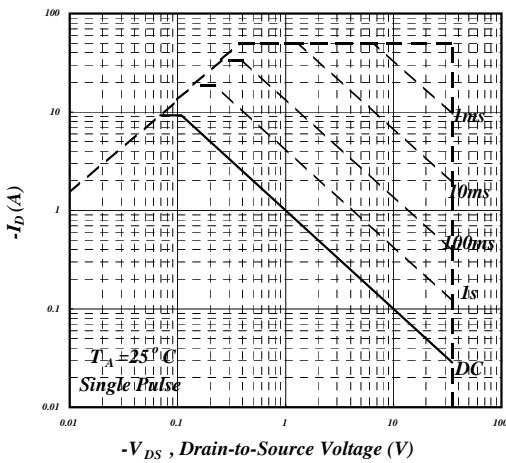


Fig 9. Maximum Safe Operating Area

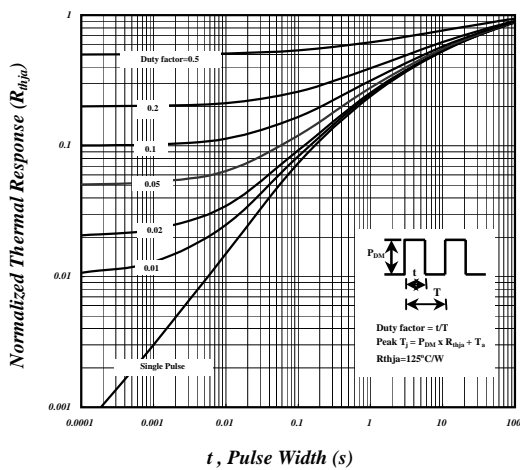


Fig 10. Effective Transient Thermal Impedance

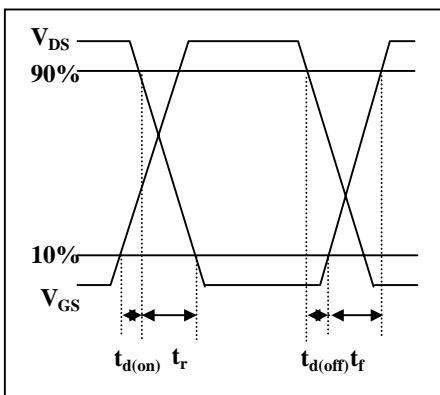


Fig 11. Switching Time Waveform

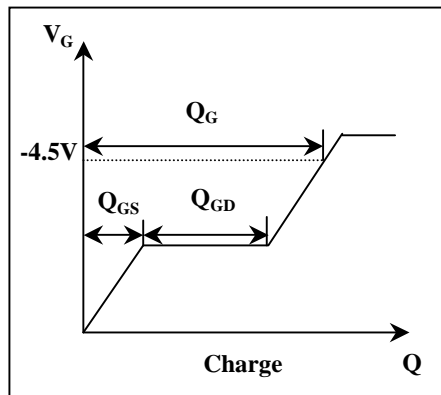


Fig 12. Gate Charge Waveform