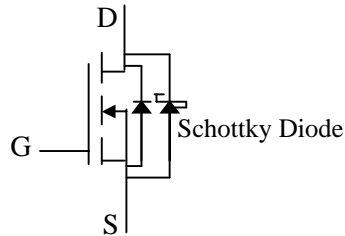




- ▼ Simple Drive Requirement
- ▼ Small Size & Lower Profile
- ▼ RoHS Compliant & Halogen-Free

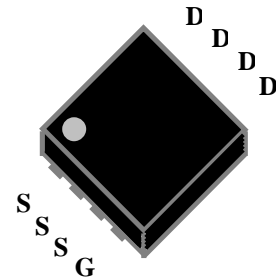


BV_{DSS}	30V
$R_{DS(ON)}$	9m Ω
I_D	15A

Description

AP6680S series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK[®] 3x3 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.



PMPAK[®] 3x3

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	+20	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current ³	15	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current ³	12	A
I_{DM}	Pulsed Drain Current ¹	50	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	3.13	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	5	$^\circ\text{C}/\text{W}$
Rthj-a	Maximum Thermal Resistance, Junction-ambient ³	40	$^\circ\text{C}/\text{W}$



AP6680SGYT-HF

Electrical Characteristics @T_J=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =12A	-	6.7	9	mΩ
		V _{GS} =4.5V, I _D =8A	-	11.2	15	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	1.45	3	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =12A	-	20	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =12A	-	10	16	nC
Q _{gs}	Gate-Source Charge	V _{DS} =15V	-	3	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =4.5V	-	5	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V	-	10	-	ns
t _r	Rise Time	I _D =1A	-	6	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	22	-	ns
t _f	Fall Time	V _{GS} =10V	-	6.5	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	1000	1600	pF
C _{oss}	Output Capacitance	V _{DS} =15V	-	225	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	150	-	pF
R _g	Gate Resistance	f=1.0MHz	-	1.9	3.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Diode+Schottky Forward On Voltage ²	I _S =1.0A, V _{GS} =0V	-	0.48	0.5	V
t _{rr}	Body Diode+Schottky Reverse Recovery Time	I _S =12A, V _{GS} =0V,	-	18	-	ns
Q _{rr}	Body Diode+Schottky Reverse Recovery Charge	di/dt=100A/μs	-	8	-	nC

Notes:

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² 2oz copper pad of FR4 board, t_≤10sec ; 210°C/W when mounted on min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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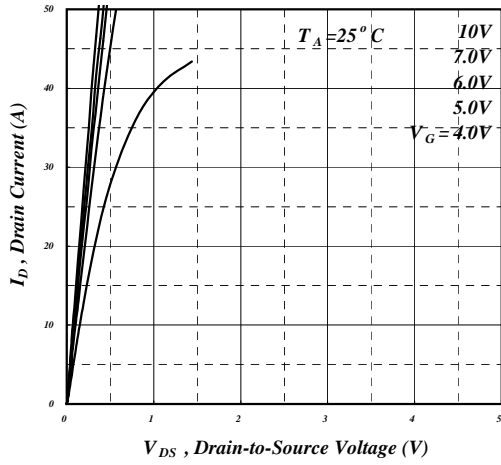


Fig 1. Typical Output Characteristics

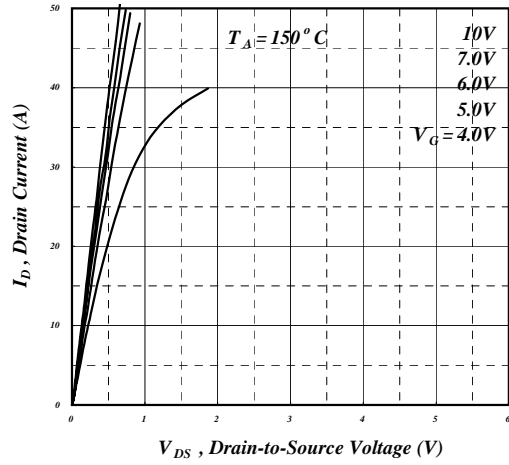


Fig 2. Typical Output Characteristics

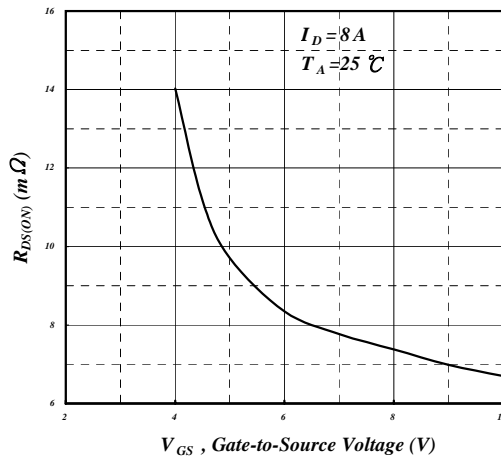


Fig 3. On-Resistance v.s. Gate Voltage

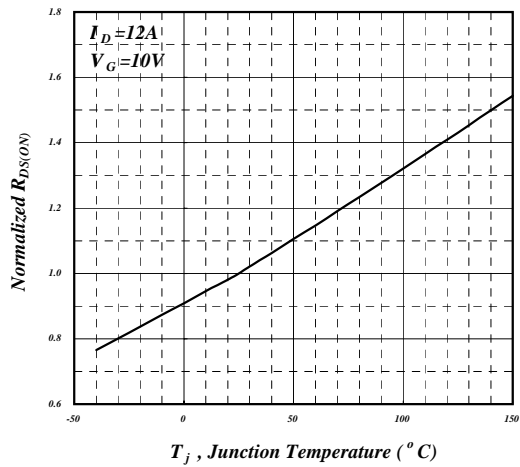


Fig 4. Normalized On-Resistance v.s. Junction Temperature

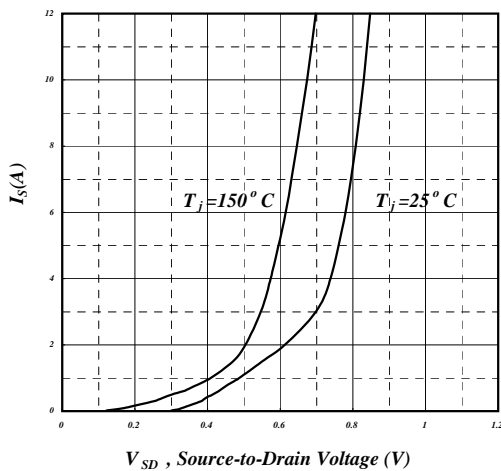


Fig 5. Forward Characteristic of Reverse Diode

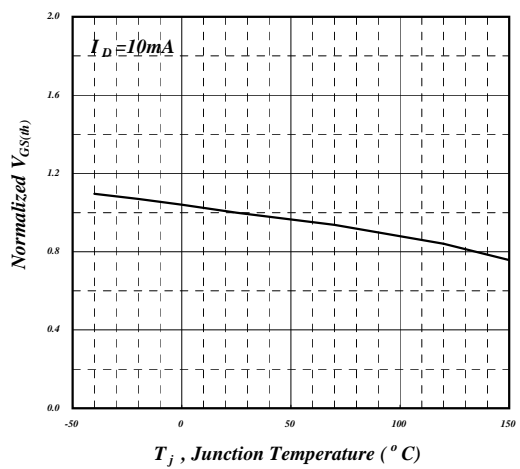


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

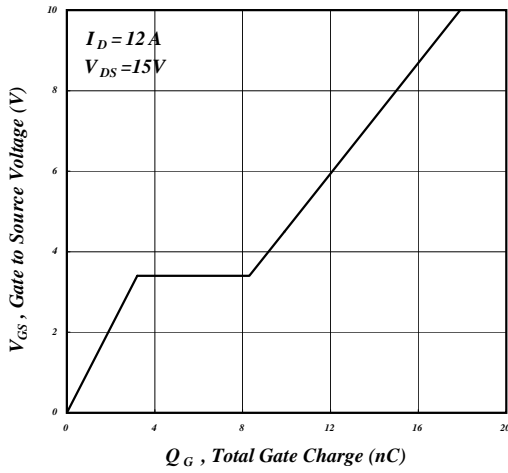


Fig 7. Gate Charge Characteristics

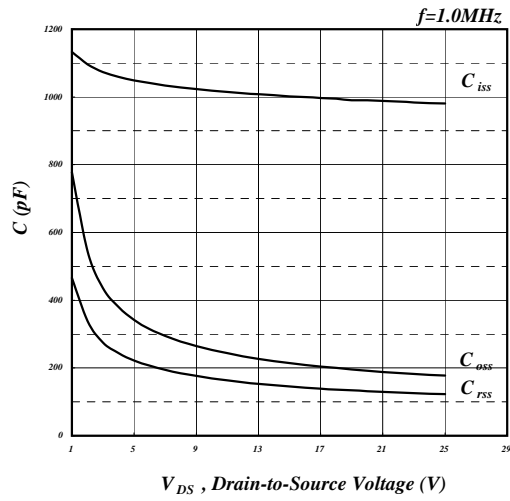


Fig 8. Typical Capacitance Characteristics

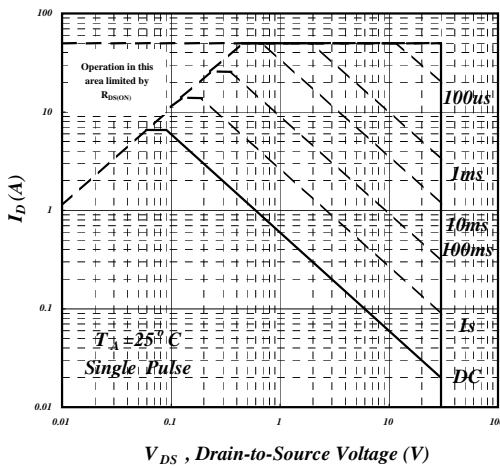


Fig 9. Maximum Safe Operating Area

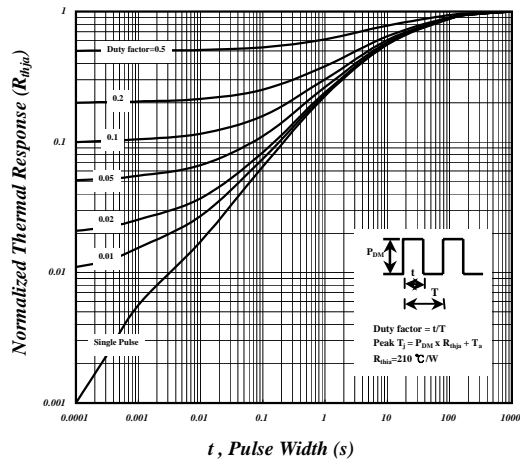


Fig 10. Effective Transient Thermal Impedance

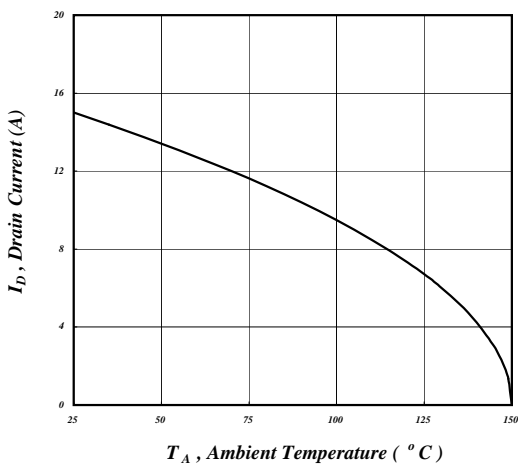


Fig 11. Maximum Continuous Drain Current v.s. Ambient Temperature



Fig 12. Gate Charge Waveform