



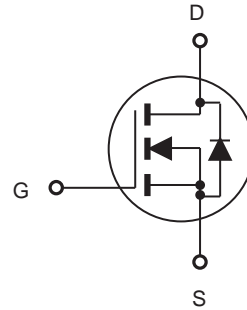
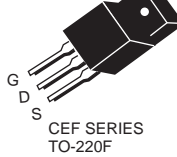
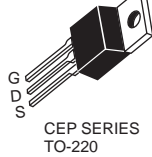
# CEP10N4/CEB10N4 CEI10N4/CEF10N4

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP10N4	450V	0.7Ω	10A	10V
CEB10N4	450V	0.7Ω	10A	10V
CEI10N4	450V	0.7Ω	10A	10V
CEF10N4	450V	0.7Ω	10A <sup>e</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- Lead free product is acquired.
- TO-220 & TO-263 & TO-262 package & TO-220F full-pak for through hole.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263/262	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	450		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current-Continuous	I <sub>D</sub>	10	10 <sup>e</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>f</sup>	40	40 <sup>e</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	125	45	W
		1.0	0.36	W/°C
Single Pulsed Avalanche Energy <sup>d</sup>	E <sub>AS</sub>	450	450	mJ
Single Pulsed Avalanche Current <sup>d</sup>	I <sub>AS</sub>	10	10	A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.0	2.8	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W



# CEP10N4/CEB10N4 CEI10N4/CEF10N4

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

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Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	450			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 450V, V_{GS} = 0V$		25	100	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$		100	500	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$		-100	-500	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6A$		0.6	0.7	$\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS} = 50V, I_D = 6A$	3	6		S
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1400		pF
Output Capacitance	$C_{oss}$			330		pF
Reverse Transfer Capacitance	$C_{rss}$			120		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200V, I_D = 10A, V_{GS} = 10V, R_{GEN} = 9.1\Omega$		14	75	ns
Turn-On Rise Time	$t_r$			27	125	ns
Turn-Off Delay Time	$t_{d(off)}$			50	100	ns
Turn-Off Fall Time	$t_f$			24	60	ns
Total Gate Charge	$Q_g$	$V_{DS} = 320V, I_D = 10A, V_{GS} = 10V$		48	65	nC
Gate-Source Charge	$Q_{gs}$			4		nC
Gate-Drain Charge	$Q_{gd}$			15		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^g$				10	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 10A$			2.0	V
<b>Notes :</b> a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . c.Guaranteed by design, not subject to production testing. d.L = 9.16mH, $I_{AS} = 10A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25^\circ\text{C}$ . e.Limited only by maximum temperature allowed . f.Pulse width limited by safe operating area . g.Full package $I_{S(max)} = 5.6A$ .						



# CEP10N4/CEB10N4 CEI10N4/CEF10N4

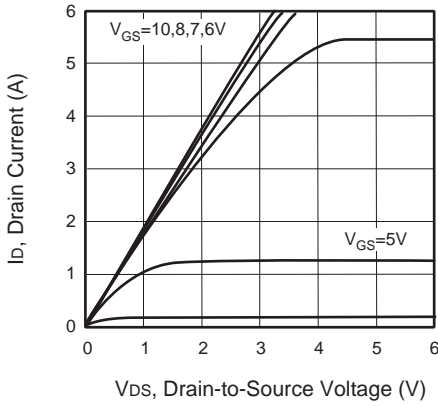


Figure 1. Output Characteristics

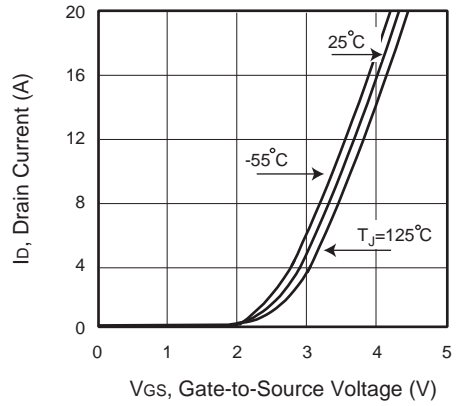


Figure 2. Transfer Characteristics

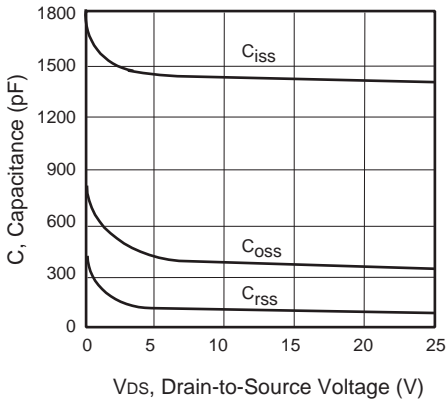


Figure 3. Capacitance

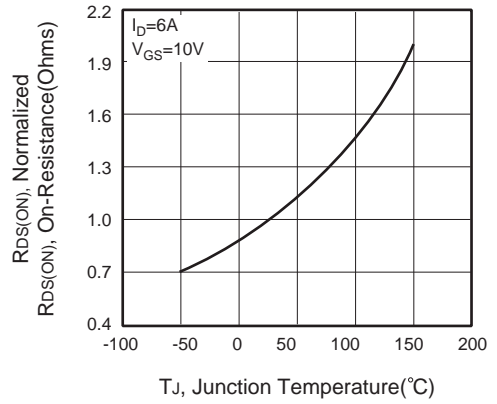


Figure 4. On-Resistance Variation with Temperature

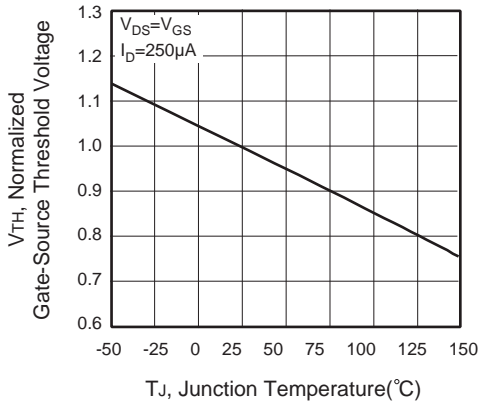


Figure 5. Gate Threshold Variation with Temperature

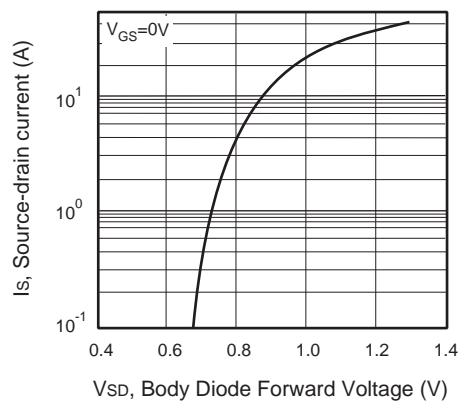


Figure 6. Body Diode Forward Voltage Variation with Source Current



# CEP10N4/CEB10N4 CEI10N4/CEF10N4

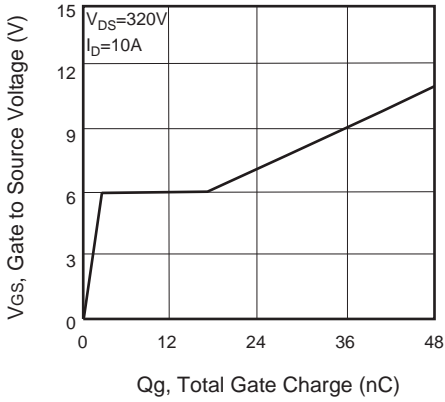


Figure 7. Gate Charge

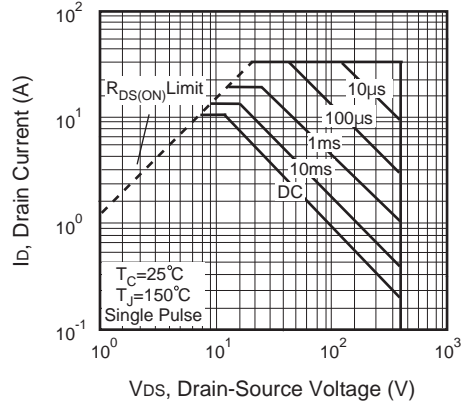


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit

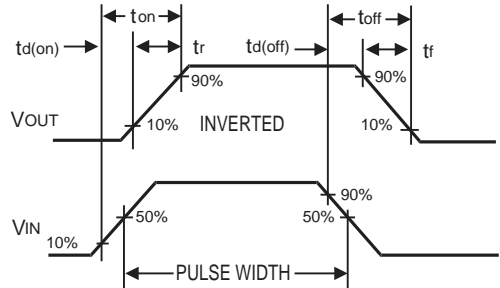


Figure 10. Switching Waveforms

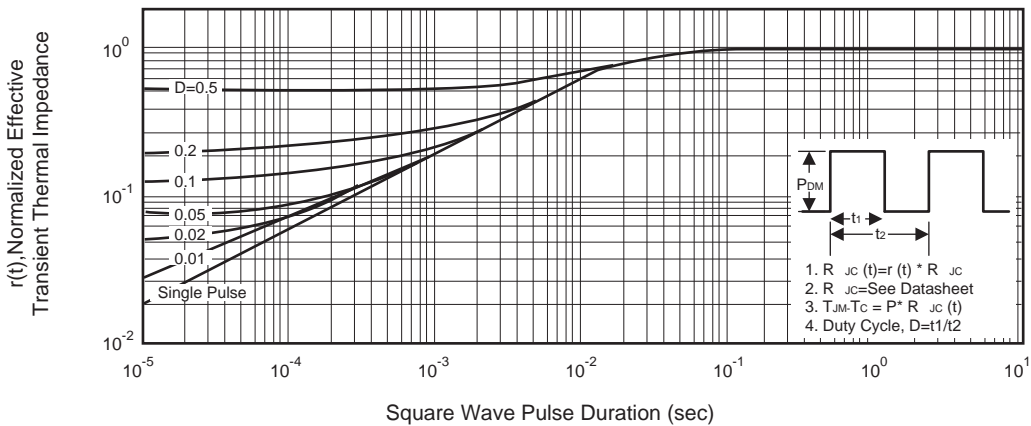


Figure 11. Normalized Thermal Transient Impedance Curve