



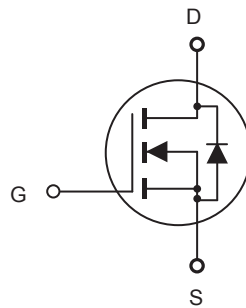
# CED07N65A/CEU07N65A

## N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

### FEATURES

- 650V, 6A,  $R_{DS(ON)} = 1.45\Omega$  @  $V_{GS} = 10V$ .
- Super high dense cell design for extremely low  $R_{DS(ON)}$ .
- High power and current handling capability.
- Lead free product is acquired.
- TO-251 & TO-252 package.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit	Units
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	V
Drain Current-Continuous @ $T_C = 25^\circ\text{C}$ @ $T_C = 100^\circ\text{C}$	$I_D$	6	A
		3.7	A
Drain Current-Pulsed <sup>a</sup>	$I_{DM}$	24	A
Maximum Power Dissipation @ $T_C = 25^\circ\text{C}$ - Derate above $25^\circ\text{C}$	$P_D$	107	W
		0.85	W/ $^\circ\text{C}$
Repetitive Avalanche Energy	$E_{AR}$	0.38	mJ
Single Pulsed Avalanche Energy <sup>e</sup>	$E_{AS}$	216	mJ
Single Pulsed Avalanche Current <sup>e</sup>	$I_{AS}$	6	A
Operating and Store Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

### Thermal Characteristics

Parameter	Symbol	Limit	Units
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.4	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	50	$^\circ\text{C/W}$

This is preliminary information on a new product in development now .  
Details are subject to change without notice .

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<http://www.cetsemi.com>



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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	650			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 650V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 3A$		1.22	1.45	$\Omega$
Gate input resistance	$R_g$	f=1MHz, open Drain		1.5		$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1410		pF
Output Capacitance	$C_{oss}$			115		pF
Reverse Transfer Capacitance	$C_{rss}$			15		pF
Effective output capacitance <sup>f</sup> energy related	$C_{o(er)}$	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 480V$		42		pF
Effective output capacitance <sup>g</sup> time related	$C_{o(tr)}$			38.5		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300V, I_D = 6A, V_{GS} = 10V, R_{GEN} = 25\Omega$		26	52	ns
Turn-On Rise Time	$t_r$			58	116	ns
Turn-Off Delay Time	$t_{d(off)}$			85	170	ns
Turn-Off Fall Time	$t_f$			63	126	ns
Total Gate Charge	$Q_g$	$V_{DS} = 480V, I_D = 6A, V_{GS} = 10V$		28	36	nC
Gate-Source Charge	$Q_{gs}$			6		nC
Gate-Drain Charge	$Q_{gd}$			9		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				5	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 5A$			1.5	V
<b>Notes :</b> a. Repetitive Rating : Pulse width limited by maximum junction temperature. b. Device Mounted on FR4 Board, $t < 10$ sec. c. Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . d. Guaranteed by design, not subject to production testing. e. $L = 12mH, I_{AS} = 6A, V_{DD} = 50V, R_G = 25\Omega$ , Starting $T_J = 25\text{ C}$ . f. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as $C_{oss}$ while $V_{ds}$ is rising from 0 to 80% $V_{dss}$ . g. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{ds}$ is rising from 0 to 80% $V_{dss}$ .						



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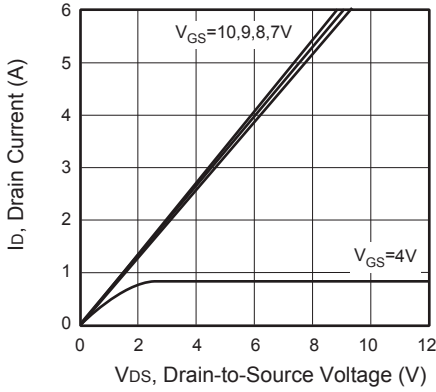


Figure 1. Output Characteristics

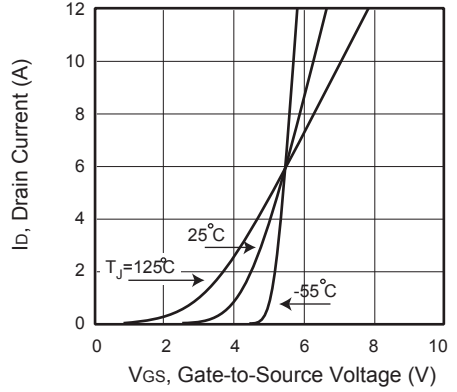


Figure 2. Transfer Characteristics

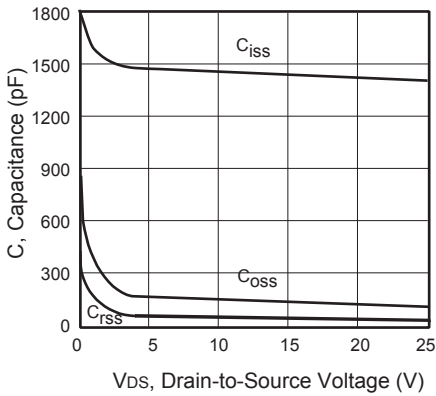


Figure 3. Capacitance

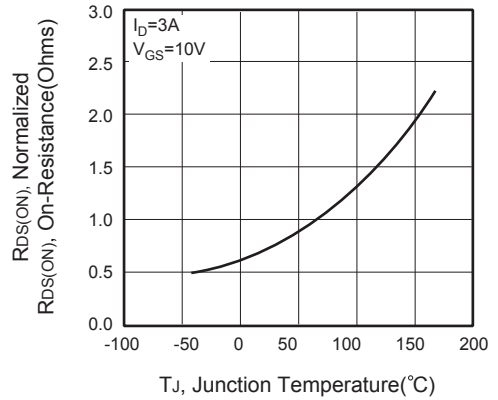


Figure 4. On-Resistance Variation with Temperature

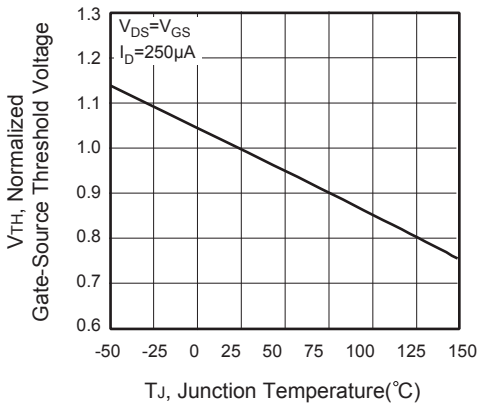


Figure 5. Gate Threshold Variation with Temperature

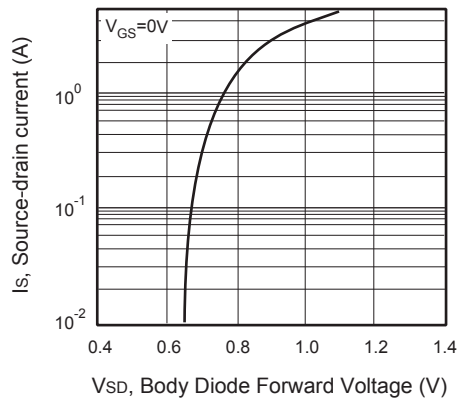


Figure 6. Body Diode Forward Voltage Variation with Source Current



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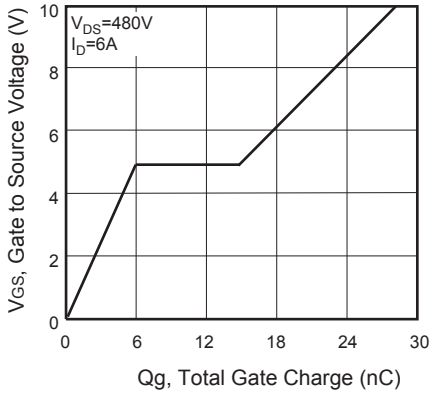


Figure 7. Gate Charge

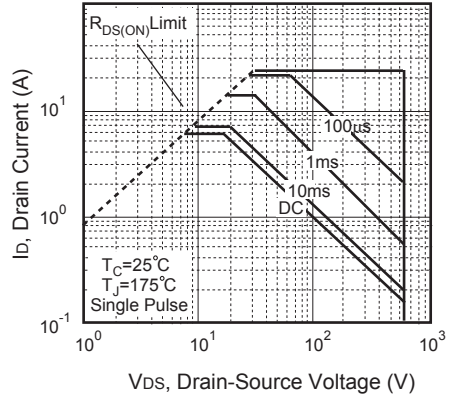


Figure 8. Maximum Safe Operating Area

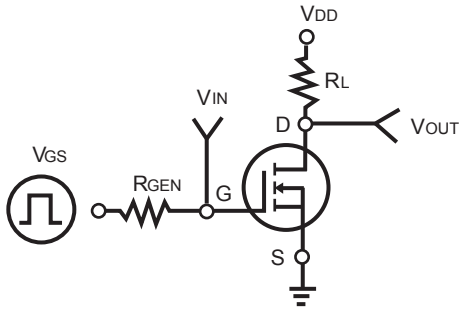


Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

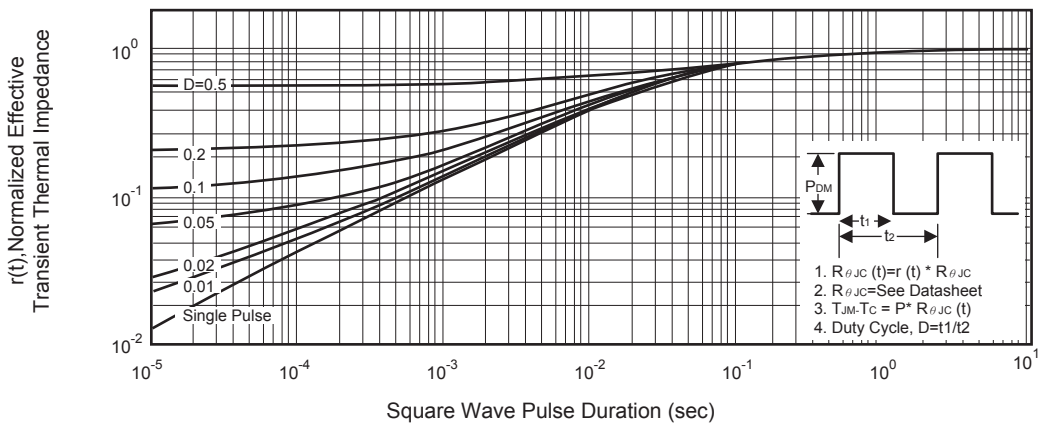


Figure 11. Normalized Thermal Transient Impedance Curve