



CEP840L/CEB840L

CEF840L

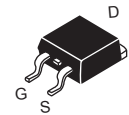
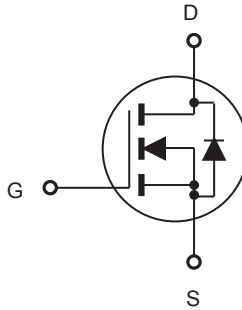
N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

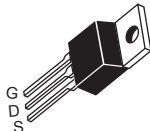
FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP840L	500V	0.8Ω	8A	10V
CEB840L	500V	0.8Ω	8A	10V
CEF840L	500V	0.8Ω	8A ^e	10V

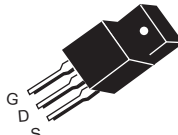
- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- Lead free product is acquired.



CEB SERIES
TO-263(DD-PAK)



CEP SERIES
TO-220



CEF SERIES
TO-220F

ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V _{DS}	500		V
Gate-Source Voltage	V _{GS}	±20		V
Drain Current-Continuous	I _D	8	8 ^e	A
Drain Current-Pulsed ^a	I _{DM} ^f	32	32 ^e	A
Maximum Power Dissipation @ T _C = 25°C - Derate above 25°C	P _D	125	40	W
		1.0	0.32	W/°C
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	1.0	3.1	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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<http://www.cetsemi.com>



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	500			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500V, V_{GS} = 0V$			25	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 20V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -20V, V_{DS} = 0V$			-100	nA
On Characteristics^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 4.8A$		0.6	0.8	Ω
Forward Transconductance	g_{FS}	$V_{DS} = 50V, I_D = 4.8A$		7		S
Dynamic Characteristics^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1240		pF
Output Capacitance	C_{oss}			145		pF
Reverse Transfer Capacitance	C_{rss}			20		pF
Switching Characteristics^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250V, I_D = 8A, V_{GS} = 10V, R_{GEN} = 9.1\Omega$		20	40	ns
Turn-On Rise Time	t_r			9	18	ns
Turn-Off Delay Time	$t_{d(off)}$			48	92	ns
Turn-Off Fall Time	t_f			8	16	ns
Total Gate Charge	Q_g	$V_{DS} = 400V, I_D = 8A, V_{GS} = 10V$		33	43.8	nC
Gate-Source Charge	Q_{gs}			6.2		nC
Gate-Drain Charge	Q_{gd}			13.9		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				8	A
Drain-Source Diode Forward Voltage ^b	V_{SD}	$V_{GS} = 0V, I_S = 8A$			1.5	V
Notes : □ a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. □ c.Guaranteed by design, not subject to production testing. □ d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)} = 4.6A$.						



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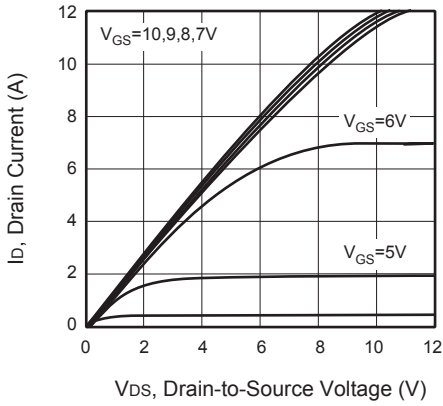


Figure 1. Output Characteristics

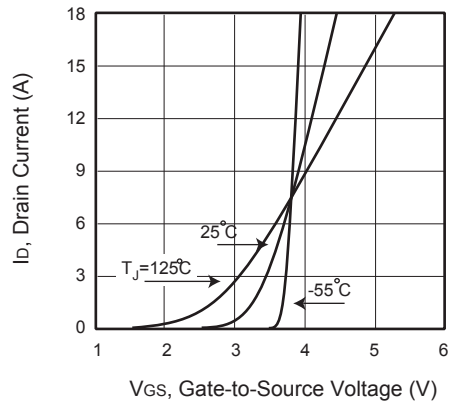


Figure 2. Transfer Characteristics

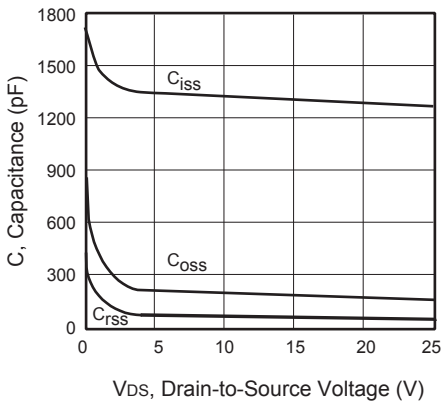


Figure 3. Capacitance

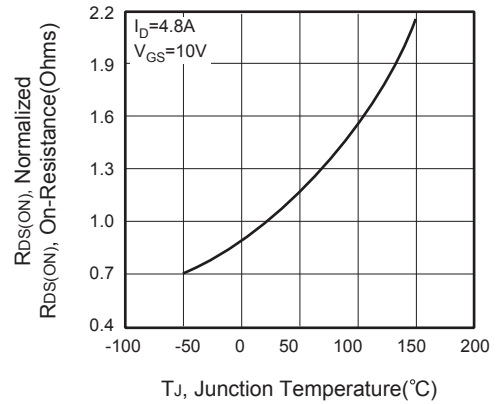


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

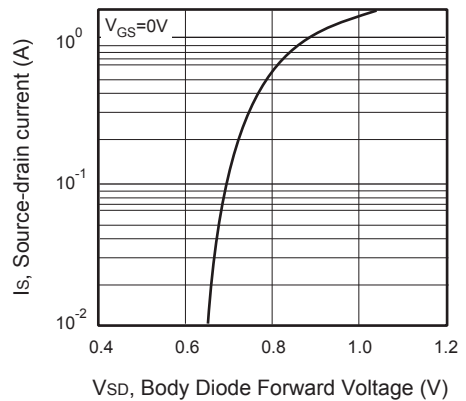


Figure 6. Body Diode Forward Voltage Variation with Source Current



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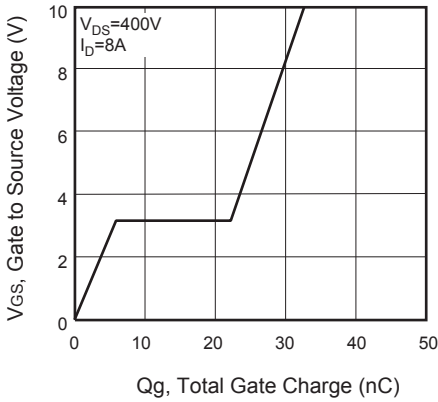


Figure 7. Gate Charge

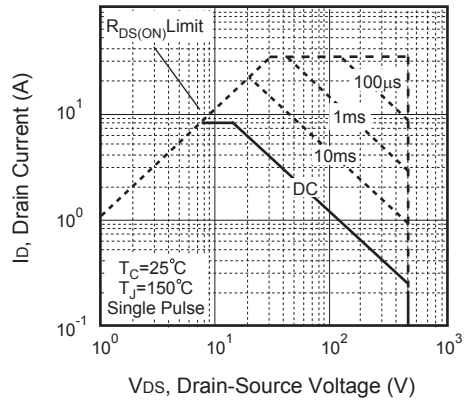


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

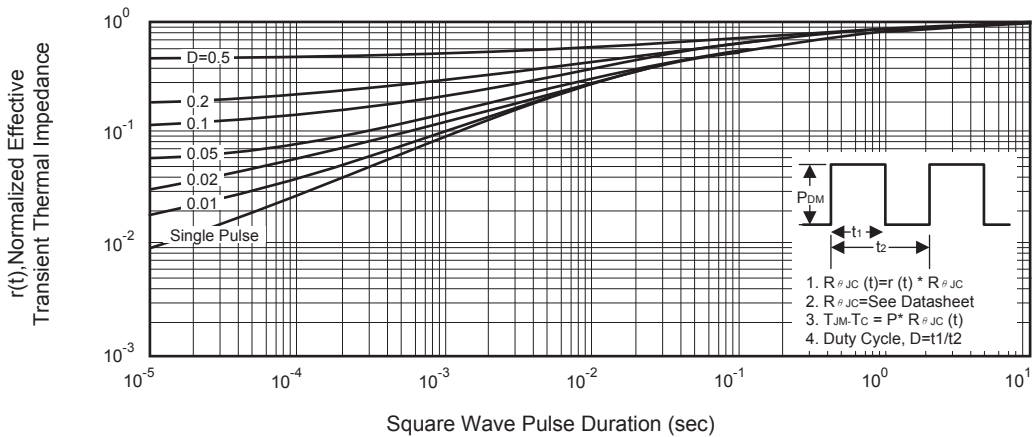


Figure 11. Normalized Thermal Transient Impedance Curve