



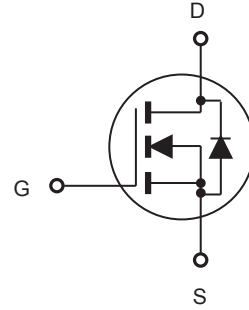
CEP6036/CEB6036

N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

- 60V, 135A, $R_{DS(ON)} = 4.6m\Omega$ @ $V_{GS} = 10V$.
- Super high dense cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.
- TO-220 & TO-263 package.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ C$ unless otherwise noted

| Parameter | Symbol | Limit | Units |
|---|----------------|------------|--------------------|
| Drain-Source Voltage | V_{DS} | 60 | V |
| Gate-Source Voltage | V_{GS} | ± 20 | V |
| Drain Current-Continuous @ $T_C = 25^\circ C$ @ $T_C = 100^\circ C$ | I_D | 135 95 | A A |
| Drain Current-Pulsed ^a | I_{DM} | 540 | A |
| Maximum Power Dissipation @ $T_C = 25^\circ C$ - Derate above $25^\circ C$ | P_D | 167 1.1 | W W/ $^\circ C$ |
| Single Pulsed Avalanche Energy ^d | E_{AS} | 400 | mJ |
| Single Pulsed Avalanche Current ^d | I_{AS} | 40 | A |
| Operating and Store Temperature Range | T_J, T_{stg} | -55 to 175 | $^\circ C$ |

Thermal Characteristics

| Parameter | Symbol | Limit | Units |
|---|-----------------|-------|--------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 0.9 | $^\circ C/W$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 62.5 | $^\circ C/W$ |

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Test Condition | Min | Typ | Max | Units |
|---|--------------|---|-----|------|------|------------|
| Off Characteristics | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | $V_{GS} = 0V, I_D = 250\mu A$ | 60 | | | V |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 60V, V_{GS} = 0V$ | | | 1 | μA |
| Gate Body Leakage Current, Forward | I_{GSSF} | $V_{GS} = 20V, V_{DS} = 0V$ | | | 100 | nA |
| Gate Body Leakage Current, Reverse | I_{GSSR} | $V_{GS} = -20V, V_{DS} = 0V$ | | | -100 | nA |
| On Characteristics^b | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{GS} = V_{DS}, I_D = 250\mu A$ | 2 | | 4 | V |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | $V_{GS} = 10V, I_D = 30A$ | | 3.7 | 4.6 | m Ω |
| Gate input resistance | R_g | f=1MHz, open Drain | | 1.9 | | Ω |
| Dynamic Characteristics^c | | | | | | |
| Input Capacitance | C_{iss} | $V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$ | | 6145 | | pF |
| Output Capacitance | C_{oss} | | | 450 | | pF |
| Reverse Transfer Capacitance | C_{rss} | | | 300 | | pF |
| Switching Characteristics^c | | | | | | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 30V, I_D = 30A,$ $V_{GS} = 10V, R_{GEN} = 3.6\Omega$ | | 34 | 68 | ns |
| Turn-On Rise Time | t_r | | | 23 | 46 | ns |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 82 | 164 | ns |
| Turn-Off Fall Time | t_f | | | 25 | 50 | ns |
| Total Gate Charge | Q_g | $V_{DS} = 48V, I_D = 30A,$ $V_{GS} = 10V$ | | 138 | 179 | nC |
| Gate-Source Charge | Q_{gs} | | | 34 | | nC |
| Gate-Drain Charge | Q_{gd} | | | 46 | | nC |
| Drain-Source Diode Characteristics and Maximum Ratings | | | | | | |
| Drain-Source Diode Forward Current | I_S | | | | 135 | A |
| Drain-Source Diode Forward Voltage ^b | V_{SD} | $V_{GS} = 0V, I_S = 30A$ | | | 1.2 | V |
| Notes: □ a. Repetitive Rating : Pulse width limited by maximum junction temperature b. Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. □ c. Guaranteed by design, not subject to production testing. □ d. L = 0.5mH, $I_{AS} = 40A$, $V_{DD} = 24V$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$ | | | | | | |



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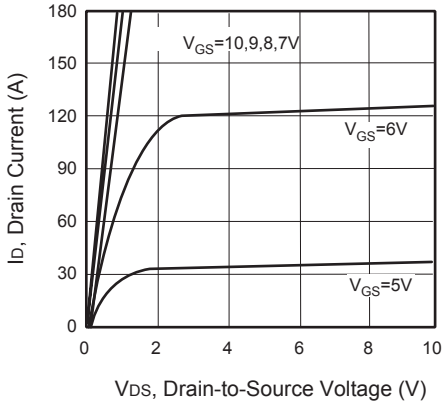


Figure 1. Output Characteristics

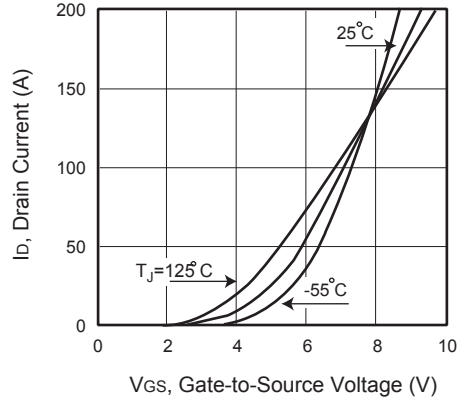


Figure 2. Transfer Characteristics

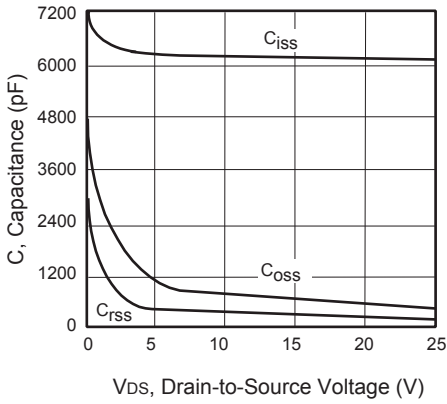


Figure 3. Capacitance

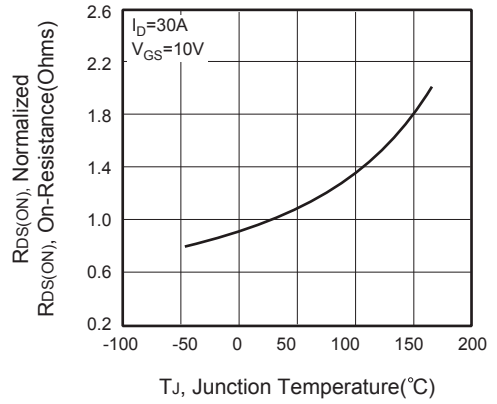


Figure 4. On-Resistance Variation with Temperature

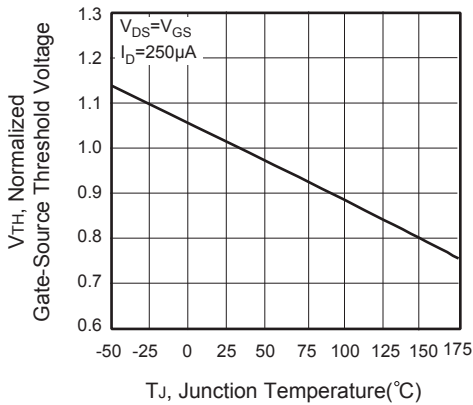


Figure 5. Gate Threshold Variation with Temperature

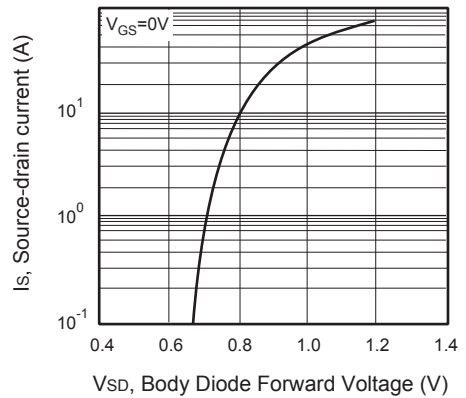


Figure 6. Body Diode Forward Voltage Variation with Source Current



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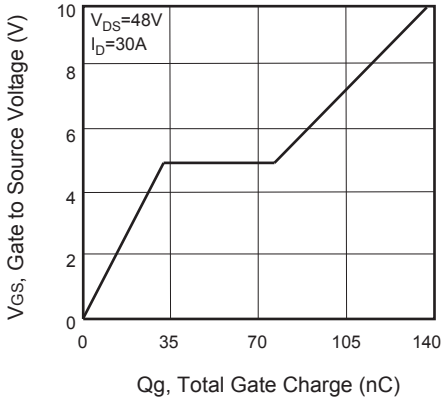


Figure 7. Gate Charge

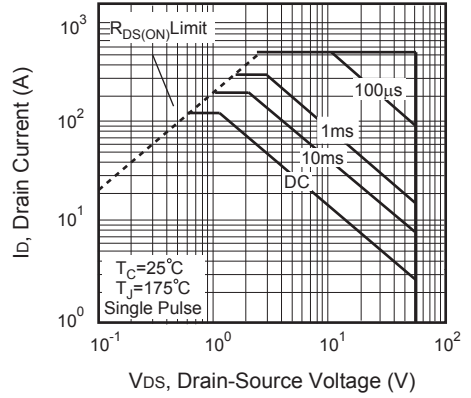


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

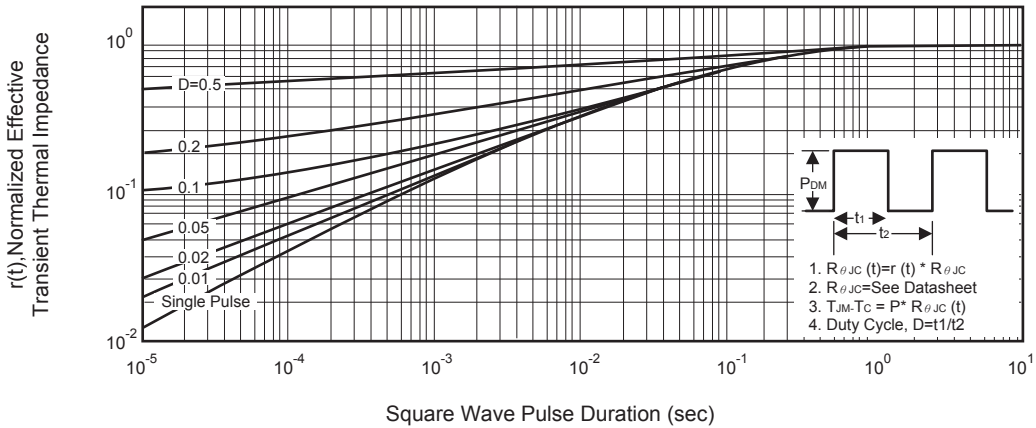


Figure 11. Normalized Thermal Transient Impedance Curve