



# CEP13N5A/CEB13N5A CEF13N5A

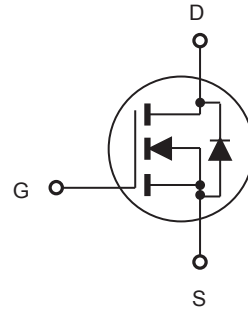
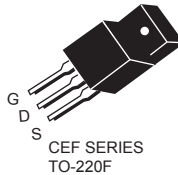
## N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP13N5A	500V	0.48Ω	13A	10V
CEB13N5A	500V	0.48Ω	13A	10V
CEF13N5A	500V	0.48Ω	13A <sup>d</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	500		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current-Continuous @ T <sub>C</sub> = 25°C @ T <sub>C</sub> = 100°C	I <sub>D</sub>	13	13 <sup>d</sup>	A
		8	8 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	52	52 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25°C - Derate above 25°C	P <sub>D</sub>	208	52	W
		1.7	0.4	W/°C
Single Pulsed Avalanche Energy <sup>h</sup>	E <sub>AS</sub>	542		mJ
Single Pulsed Avalanche Current <sup>h</sup>	I <sub>AS</sub>	8.5		A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	0.6	2.4	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	65	°C/W

This is preliminary information on a new product in development now .  
Details are subject to change without notice .

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<http://www.cetsemi.com>



# CEP13N5A/CEB13N5A CEF13N5A

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	500			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 500V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6.5A$		0.38	0.48	$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		1965		pF
Output Capacitance	$C_{oss}$			185		pF
Reverse Transfer Capacitance	$C_{rss}$			1		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250V, I_D = 13A,$ $V_{GS} = 10V, R_{GEN} = 25\Omega$		32	64	ns
Turn-On Rise Time	$t_r$			18	36	ns
Turn-Off Delay Time	$t_{d(off)}$			79	158	ns
Turn-Off Fall Time	$t_f$			16	32	ns
Total Gate Charge	$Q_g$	$V_{DS} = 400V, I_D = 13A,$ $V_{GS} = 10V$		31	40	nC
Gate-Source Charge	$Q_{gs}$			11		nC
Gate-Drain Charge	$Q_{gd}$			7		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S^f$				13	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}^g$	$V_{GS} = 0V, I_S = 13A$			1.4	V
<b>Notes :</b> □ a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . □ c.Guaranteed by design, not subject to production testing. □ d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . f.Full package $I_{S(max)}$ = 6.6A . g.Full package $V_{SD}$ test condition $I_S = 6.6A$ . □ h.L = 15mH, $I_{AS} = 8.5A$ , $V_{DD} = 50V$ , $R_G = 25\Omega$ , Starting $T_J = 25 \text{ C}$						



# CEP13N5A/CEB13N5A CEF13N5A

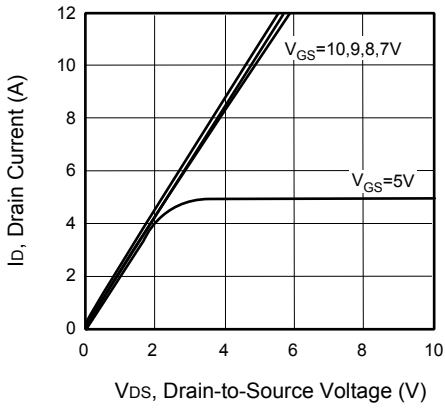


Figure 1. Output Characteristics

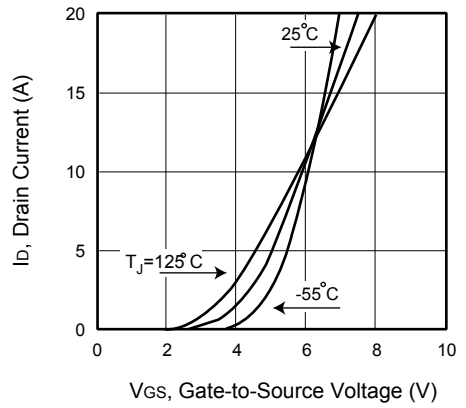


Figure 2. Transfer Characteristics

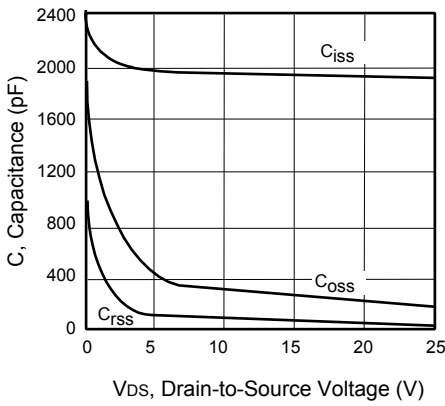


Figure 3. Capacitance

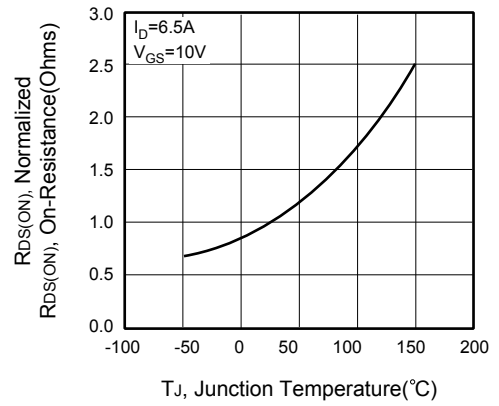


Figure 4. On-Resistance Variation with Temperature

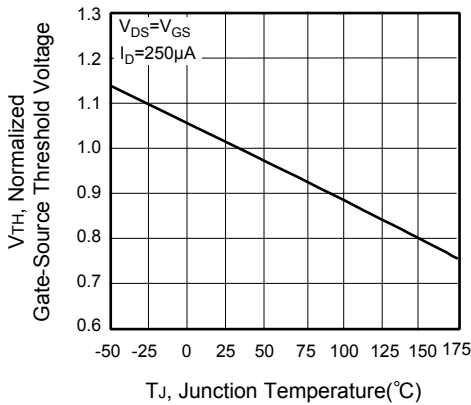


Figure 5. Gate Threshold Variation with Temperature

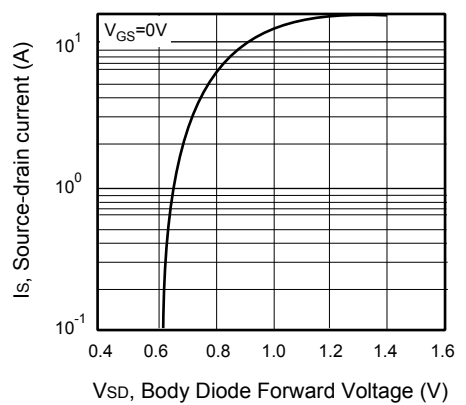


Figure 6. Body Diode Forward Voltage Variation with Source Current



# CEP13N5A/CEB13N5A CEF13N5A

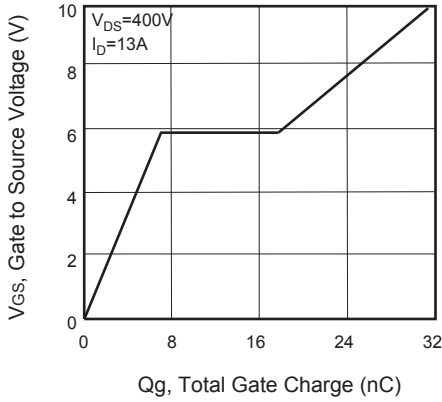


Figure 7. Gate Charge

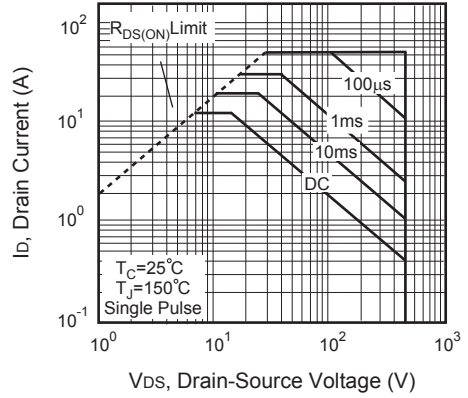


Figure 8. Maximum Safe Operating Area



Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

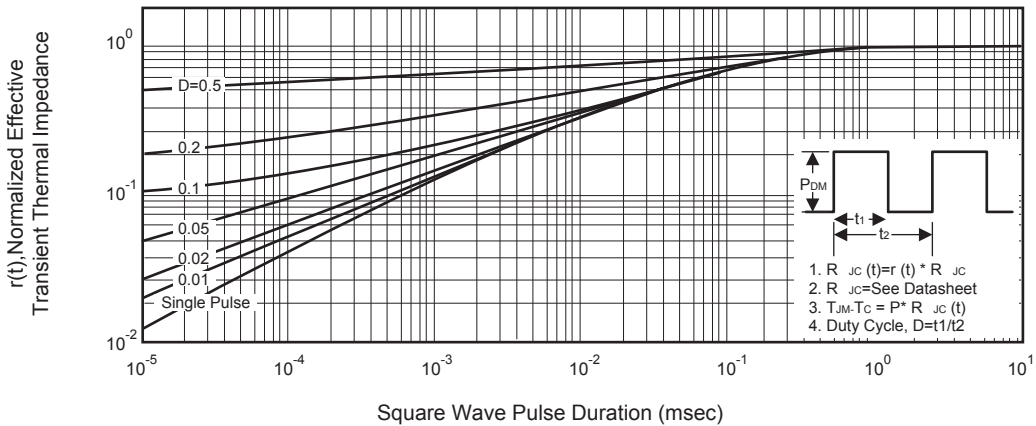


Figure 11. Normalized Thermal Transient Impedance Curve